PCI Express®
Card Electromechanical Specification
Revision 4.0, Version 0.5

~~May 23~~Septem~~Nov~~Decem~~Octo~~ber ~~18~~09~~18~~30, ~~2014~~2015

Revision	Revision History	Date
1.0	Initial release.	7/22/2002
1.0a	Incorporated WG Errata C1-C7 and E1.	4/15/2003
1.1	Incorporated approved Errata and ECNs.	3/28/2005
2.0	Added support for 5.0 GT/s data rate.	4/11/2007
3.0	• Added support for 8.0 GT/s data rate and incorporated approved Errata and ECNs. Incorporated the *PCI Express x16 Graphics 150W-ATX Specification* and the *PCI Express ~~225~~ 225 W/~~300~~ 300 W High Power Card Electromechanical Specification*. • Re-imported all figures • Updated Figure 6-1 and Figure 6-3 • Fixed text notes in Chapter 6 and 9 Figures (took notes out of Illustrator and made them part of the Word file) • Changed 306.67 MAX dimension to 326.03 MIN in Figure 9-3	7/21/2013
4.0	• Added support for 16.0 GT/s data rate and incorporated approved Errata and ECNs.	10/11/2013

~~Request for Input~~

~~For Gen 4, the CEM spec will be officially recognizing Surface Mount Technology (SMT) connectors. There is currently only information for through-hole connectors (Section 6) and equivalent information describing SMT connectors is needed. Any workgroup member who wants to provide information on SMT connectors such as layout footprint, and mechanical specifications is encouraged to do so. From this, the specification specific information will be developed.~~

Contents

Figures

Tables

1

1. Introduction

This specification is a companion for the *PCI Express Base Specification, Revision 4.0*. Its primary focus is the implementation of an evolutionary strategy with the current PCI™ desktop/server mechanical and electrical specifications. The discussions are confined to ATX or ATX-based form factors. Other form factors, such as PCI Express® Mini Card are covered in other separate specifications. This specification also provides additional capabilities for PCI Express add-in cards within the existing framework of an evolutionary strategy that is based on existing system board form factors. This specification has features designed to deliver additional electrical power to a PCI Express add-in card and provide increased card volume for the management of thermals. The *Balanced Technology Extended (BTX) Interface Specification* is acknowledged as another form factor. The support of PCI Express ~~150~~ 150 W in a BTX system was considered during the development of this specification, and it was agreed to that this version should target the ATX form factor. Expanding this specification in the future to support other form factors may be considered when compelling needs arise. As graphics power and thermal requirements have risen over time, the targeted application for this specification is broadened over the technology (AGP) that it replaces. As such, the *PCI Express 150W-ATX* portion of this specification is intended to support both workstation and consumer graphics along with other applications requiring additional power.

This specification addresses only the single card scenario for ~~150~~ 150 W, ~~225~~ 225 W, and ~~300~~ 300 W cards. It is expected that, with tight cooperation between graphics card vendors or other high power card vendors and system OEMs, systems can scale and support multiple high power cards in a modular fashion.

This specification supports five distinct maximum power levels for add-in cards: ~~25~~ 25 W (low profile card), ~~75~~ 75 W (standard size), ~~150~~ 150 W, ~~225~~ 225 W, ~~and~~ and 300 W. In order to achieve maximum interoperability and a non-compromised end user experience, intermediate power levels leveraging optional components of *PCI Express Base Specification~~, Revision 4.0~~* are outside the scope of the PCI Express electromechanical specification.

This specification does not support the optional hot-plug functionality for ~~150~~ 150 W, ~~225~~ 225 W, or ~~300~~ 300 W cards, nor does it preclude such support using an implementation-specific method.

1.1. Terms and Definitions

add-in card	A card that is plugged into a connector and mounted in a chassis slot.
AIC	Add-in card.
AGP	Accelerated Graphics Port.
ATX	A system board form factor. Refer to the ATX Specification, Revision. 2.2.
~~**ATX-based form**~~	
ATX-based form factor	Refers to the form factor that does not exactly conform to the ATX specification, but uses the key features of ~~the~~ ATX, such as the slot spacing, I/O panel definition, etc.
Auxiliary signals	Signals ~~not~~, some of which are ~~required by~~defined in the PCI Express ~~architecture~~ Base Specification, that are used in conjunction with PCI Express signaling. Some are~~but~~ necessary for basic PCI Express operation (e.g., reference clock and reset) ~~certain desired functions or system implementation, for example~~while others provide ancillary capabilities (e.g., the SMBus signals). See also Sideband signaling.
Basic bandwidth	Contains one PCI Express Lane.
x1, x2, x4, x8,	
x12, x16	x1 refers to one PCI Express Lane of basic bandwidth; x4 refers to a collection of four PCI Express Lanes; etc.
Card	A card that is plugged into a connector and mounted in a chassis slot.
Card Interoperability	Ability to plug a PCI Express card into different Link width connectors and the system works, for example, plugging a ~~PCI Express~~ x1 card into a x16 slot.
CEM	Card Electromechanical.
Down-plugging	Plugging a larger Link mechanical width card into a smaller Link mechanical width connector, for example, plugging a x4 card into a x1 connector.
DUAL-SLOT Card	A card that plugs into a single edge connector – but whose volume occupies a total of two adjacent expansion slots.
ECN	Engineering Change Notice.
Evolutionary strategy	A strategy to develop the PCI Express connector and card form factors within today's chassis and system board form factor infrastructure constraints.
High bandwidth	Supports a larger number of PCI Express Lanes, such as a x16 card or connector.
HE	High-End.
Hot-Plug	Insertion and/or removal of a card into an active backplane or system board as defined in PCI Standard Hot-Plug Controller and Subsystem Specification, Revision. 1.0. No special card support is required.
Hot swap	Insertion and/or removal of a card into a passive backplane. The card must satisfy specific requirements to support Hot swap.
Link	A collection of one or more PCI Express Lanes.
Low profile card	An add-in card whose height is no more than 68.90 mm (2.731 inches).
microATX	An ATX-based system board form factor. Refer to the microATX Motherboard Interface Specification, Revision 1.2.
PCIe	PCI Express.
PCI Express Lane	One PCI Express Lane contains two differential lines for Transmitter and two differential lines for Receiver. A xN Link is composed of N Lanes.
PCI Express Mini	PCI Express for mobile form factor, similar to Mini PCI. Refer to the PCI Express Mini Card

Card	Electromechanical Specification.
Receiver path	The path from the connector to the receiver for a differential data pair (system) or the edge finger to the receiver (add-in card).
REFCLK	The reference clock differential pair consisting of auxiliary signals REFCLK+ and REFCLK-.
SINGLE-SLOT Card	A card that uses a single expansion slot.
sideband signaling	A method for signaling events and conditions using physical signals separate from signals forming the Link between two components. See also Auxiliary signals.
Standard height card	An add-in card whose maximum height is no more than 111.28 mm (4.381 inches).
Transmitter path	The path from the transmitter to the connector for a differential data pair (system) or the transmitter to the edge finger (add-in card).
TRIPLE-SLOT Card	A card that plugs into a single edge connector – but whose volume occupies a total of three adjacent expansion slots.
Up-plugging	Plugging a smaller Link mechanical width card into a larger Link mechanical width connector, for example, plugging a x1 card into a x4 connector.
wakeup	A mechanism used by a component to request the reapplication of main power when in the L2 Link state. Two such mechanisms are defined in the PCI Express Base Specification: Beacon and WAKE#. This specification requires the use of WAKE# on any add-in card or system board that supports wakeup functionality.

1.2. Reference Documents

This specification references the following documents:

- PCI Express Base Specification, Revision 4.0
- PCI Local Bus Specification, Revision 3.0
- ~~PCI Local Bus Specification, Revision 3.0 (Is this being moved into the base spec?~~
- PCI Express Jitter Modeling
- PCI Express Jitter and BER
- ATX Specification, Revision 2.2
- microATX Motherboard Interface Specification, Revision 1.2
- SMBus Specification, Revision 2.0
- ~~JTAG Specification (IEEE1149.1)~~IEEE Standard 1149.1, Test Access Port and Boundary Scan Architecture
- PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0
- PCI Hot-Plug Specification, Revision 1.1
- Compact PCI Hot Swap Specification
- EIA-364-1000.01: Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications
- EIA-364: Electrical Connector/Socket Test Procedures Including Environmental Classifications

Formatted: Font: Not Italic

Formatted: Bulleted + Level: 1 + Aligned at: 0.25" + Indent at: 0.5"

Formatted: Font: Not Italic

Formatted: Indent: Left: 0.25"

Formatted: Font: Not Italic

Formatted: Bulleted + Level: 1 + Aligned at: 0.25" + Indent at: 0.5"

- ISO 3744, Acoustics – Determination of Sound Power Levels of Noise Sources Using Sound Pressure – Engineering Method in an Essentially Free Field Over a Reflecting Plane
- ISO 7779, Acoustics – Measurement of Airborne Noise Emitted by Information Technology and Telecommunications Equipment
- PCI Bus Power Management Interface Specification, Revision 1.2
- PCI Express Label Specification
- PHY Electrical Test Considerations for PCI Express Architecture
- Balanced Technology Extended (BTX) Interface Specification
- PCI Express Mini-CEM Specification, Revision 1.0
- PCI Bus Power Management Interface Specification
- PCI Express Graphics Card Thermal Mechanical Design Guidelines
- EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA 364-90 – Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- EIA 364-108 – Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems
- PCI Express Connector High Speed Electrical Test Procedure

Formatted: Font color: Black
Formatted: Font: Not Italic, Not Highlight
Formatted: Font: Not Italic
Formatted: Font: Not Italic, Not Highlight
Formatted: Font: Not Italic
Formatted: Font: (Default) Garamond, 12 pt
Formatted: Font: Not Italic
Formatted: Font color: Black
Formatted: Font: Not Italic
Formatted: Font color: Black
Formatted: Font color: Black
Formatted: Font: Not Italic
Formatted: Font color: Black
Formatted: Font: Not Italic
Formatted: Font color: Black
Formatted: Font: Not Italic
Formatted: Bulleted + Level: 1 + Aligned at: 0.25" + Indent at: 0.5"

1.3. Specification Contents

This specification contains the following information:

- Auxiliary signals
- Add-in card hot insertion and removal
- Power delivery
- Add-in card electrical budget
- Connector specification
- Card form factors and implementation
- System requirements
- Supplemental power connector specification

1.4. Objectives

The objectives of this specification are:

- Support 16.0 GT/s, 8.0 GT/s, 5.0 GT/s and 2.5 GT/s data rate (per direction)
- Enable Hot-Plug and hot swap where they are needed
- Leverage desktop and server commonality
- Facilitate smooth transitions
- Allow co-existence of both PCI and PCI Express add-in cards
- No chassis or other PC infrastructure changes
- Forward looking for future scalability
- Extensible for future bandwidth needs
- Allows future evolution of PC architecture
- Maximize card interoperability for user flexibility
- Low cost
- Support for PCI Express add-in cards that have higher power requirements
- Allow evolution of the PC architecture including graphics
- Upgradeability
- Enhanced end user experience

Formatted: Indent: Left: 0.25", Hanging: 0.25"

1.5. Electrical Overview

The electrical part of this specification covers auxiliary signals, hot insertion and removal, power delivery, and add-in card interconnect electrical budgets for the evolutionary strategy. The PCI Express Transmitter and Receiver electrical requirements are specified in the *PCI Express Base Specification~~, Revision 4.0~~*.

Besides the signals that are required to transmit/receive data on the PCI Express interface, there are also signals that may be necessary to implement the PCI Express interface in a system environment, or to provide certain desired functions. These signals are referred to as the auxiliary signals. They include:

- Reference clock (REFCLK-/REFCLK+), must be supplied by the system (see Section 2.1.1)
- Add-in card presence detect pins (PRSNT1# and PRSNT2#), required
- PERST#, required
- CLKREQ#, optional
- JTAG, optional
- SMBus, optional
- Wake (WAKE#), required only if the device/system supports wakeup and/or the OBFF mechanism
- Power Break (PWRBRK#), optional
- +3.3Vaux, optional

REFCLK, CLKREQ#, JTAG, SMBus, PERST#, WAKE# and PWRBRK# are described in Chapter 2; +3.3Vaux is described in Chapter 4; and PRSNT1# and PRSNT2# are described in Chapter 3.

Both Hot-Plug and hot swap of PCI Express add-in cards are supported, but their implementation is optional. Hot-Plug is supported with the evolutionary add-in card form factor. Hot swap is supported with other form factors and will be described in other specifications.

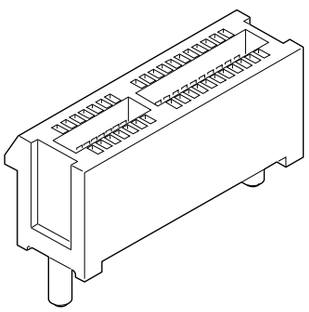
To support Hot-Plug, presence detect pins (PRSNT1# and PRSNT2#) are defined in each end of the connectors and add-in cards. The presence detect pins are staggered on the add-in cards such that they are last-mate and first-break, detecting the presence of the add-in cards. Chapter 3 discusses the detailed implementation of PCI Express Hot-Plug.

Chapter 4 specifies the PCI Express add-in card electrical requirements, which include power delivery and interconnect electrical budgets. Power is delivered to the PCI Express add-in cards via add-in card connectors, using three voltage rails: +3.3V, +3.3Vaux, and +12V. ~~Note that t~~The +3.3Vaux voltage rail is not required for all platforms (refer to Section 4.1 for more information on the required usage of 3.3Vaux). The maximum add-in card power definitions are based on the card size and Link widths, and are described in Section 4.2. Chapter 4 describes the interconnect electrical budgets, focusing on the add-in card loss and jitter requirements.

1.6. Mechanical Overview

PCI Express can be used in many different applications in desktop, mobile, server, as well as networking and communication equipment. Consequently, multiple variations of form factors and connectors will exist to suit the unique needs of these different applications.

Figure 1-1~~Figure 1-1~~~~Figure 1-1~~ shows an example of the vertical edge-card PCI Express connector to be used in ATX or ATX-based systems. There will be a family of such connectors, containing one to 16 PCI Express Lanes. The basic bandwidth (BW) version supports one PCI Express Lane and could be used as the replacement for the PCI connector. The high bandwidth version will support 16 PCI Express Lanes and will be used for applications that require higher bandwidth, such as graphics.



OM14739

Figure 1-1~~1 1~~: Vertical Edge-Card Connector

Vertical edge card connectors also have applications in the server market segment. Figure 1-2~~Figure 1-2~~~~Figure 1-2~~ shows an example of a server configuration using a PCI Express riser card.

Formatted: Font: Not Bold

Formatted: Font: Not Bold

Formatted: Font: Not Bold

Formatted: Font: Not Bold

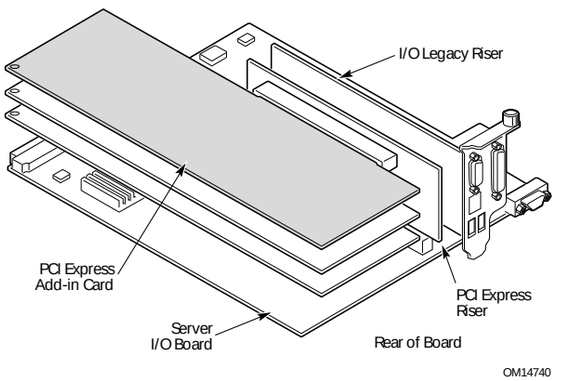


Figure 1-~~21 2~~: Example Server I/O Board with PCI Express Slots on a Riser

This specification focuses on the vertical edge card PCI Express connectors and form factor requirements by covering the following:

- Connector mating interfaces and footprints including both through-hole and surface mount technologies
- Electrical, mechanical, and reliability requirements of the connectors, including the connector testing procedures
- Add-in card form factors – including their keep-out areas within the card as well as the keep-out areas required to exit the chassis including the I/O connectors and mating cables for a typical desktop system chassis (ATX/microATX form factor).
- Connector and add-in card locations, as well as keep-outs on a typical desktop system board (ATX/microATX form factor)

Connector definitions and requirements are addressed in Chapter 6 and add-in card form factors and implementation issues are discussed in Chapter 9.

1.7. ~~150~~ 150 W Overview

A PCI Express 150W-ATX add-in card is defined as a card that consumes greater than ~~75~~ 75 W with support for up to ~~150~~ 150 W inclusive. A card that uses a single expansion slot is described as a SINGLE-SLOT add-in card. A card that extends into the adjacent expansion slot is described as a DUAL-SLOT add-in card. A card that extends into the two adjacent expansion slots is described as a TRIPLE-SLOT add-in card. A ~~150~~ 150 W add-in card, as with any CEM add-in card, may be SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT. A system that supports a PCI Express 150W-ATX add-in card is required to ensure that sufficient power and thermal support exists. For example, in an ATX form factor system, the adjacent expansion slot can be left vacant allowing for 1.37 inches of clearance for the add-in card as illustrated in Figure 1-3~~Figure 1-3~~~~Figure 1-3~~ to support a ~~150~~ 150 W or lower power DUAL-SLOT add-in card.

Formatted: Font: Not Bold

Formatted: Font: Not Bold

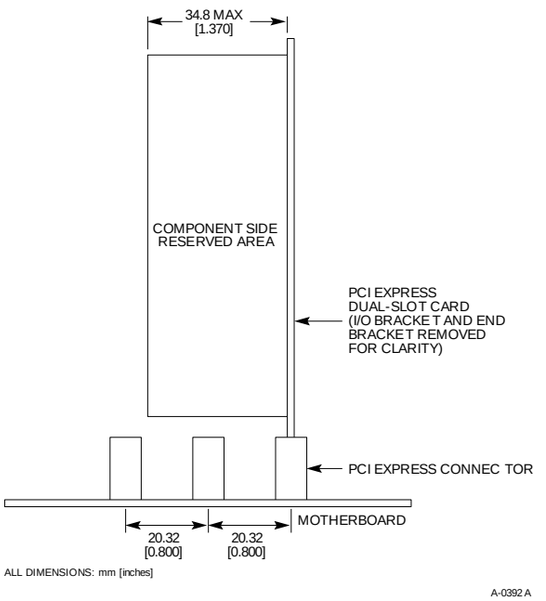


Figure 1-~~31~~ 3: Example Orientation for DUAL-SLOT Add-in Cards

A DUAL-SLOT add-in card plugs into the standard PCI Express connector but is not permitted to plug into any other adjacent add-in card connectors for any purpose.

A PCI Express 150W-ATX add-in card can draw a maximum of ~~75~~ 75 W from the standard CEM connector. Additional power, up to 75 W, is provided through an additional connector that is detailed in this specification. Therefore, the maximum power that must be provided to a PCI Express 150W-ATX add-in card is 150 W.

1.8. ~~225~~ 225 W and ~~300~~ 300 W Add-in Card Overview

A PCI Express ~~225~~ 225 W add-in card is defined as a card that exceeds PCI Express ~~150~~ 150 W ~~1.0~~ power delivery or thermal capability and, as such, consumes greater than ~~150~~ 150 W with support for up to 225 W inclusive. This card, as with any CEM add-in card, may be a SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT add-in card. A system that supports a PCI Express ~~225~~ 225 W add-in card is required to ensure that sufficient power and thermal support exists. For example, in an ATX system, the adjacent expansion slot may be left vacant allowing for 34.8 mm (1.37 inches) maximum clearance for the add-in card, as illustrated in ~~Figure 1-3~~Figure 1-3~~Figure 1-3~~. The area on the add-in card that can utilize this height, as well as the restricted height of the secondary side, is determined by the general PCI Express add-in card requirements for these dimensions.

A PCI Express ~~300~~ 300 W add-in card is defined as a card that consumes greater than ~~225~~ 225 W with support for up to ~~300~~ 300 W inclusive. This card, as with any CEM add-in card, may be a SINGLE-SLOT, DUAL-SLOT, or TRIPLE-SLOT add-in card. A system that supports a PCI Express 300 W add-in card is required to ensure that sufficient power and thermal support exists. As another example, in an ATX form factor system, the adjacent expansion slot may be left vacant allowing for 55.12- mm (2.~~17~~ 17 inches) maximum clearance for the add-in card, as illustrated in ~~Figure 1-4~~Figure 1-4~~Figure 1-4~~. The area on the add-in card that can utilize this height, as well as the restricted height of the secondary side, is determined by the general PCI Express add-in card requirements for these dimensions.

Formatted: Font: Not Bold

Formatted: Font: Not Bold

Formatted: Font: Not Bold

Formatted: Font: Not Bold

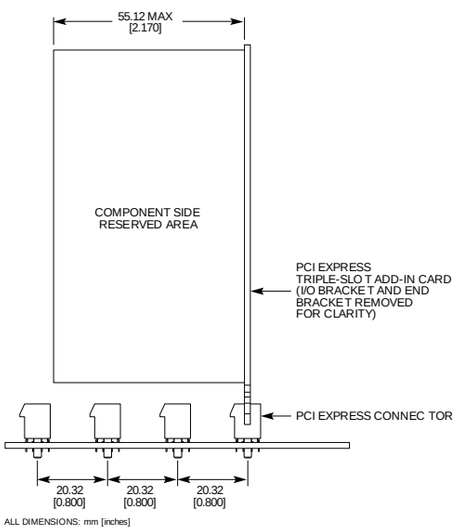


Figure 1-~~4~~1-4: Example Orientation for TRIPLE-SLOT Cards

A PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card can draw a maximum of ~~75~~ 75 W through the standard connector. Additional power, up to ~~150~~ 150 W for the ~~225~~ 225 W add-in card and up to

~~225~~ 225 W for the 300 W add-in card, is provided through additional auxiliary connector(s) that is(are) detailed in this specification.

2

2. Auxiliary Signals

The auxiliary signals are provided on the connector to assist with certain system level functionality or implementation. These signals are not required by the PCI Express architecture. The high-speed signal voltage levels are compatible with advanced silicon processes. The optional low speed signals are defined to use the +3.3V or +3.3Vaux supplies, as they are the lowest common voltage available. Most ASIC processes have high voltage (thick gate oxide) I/O transistors compatible with +. Use of the +3.3V supply allows PCI Express signaling to be used with existing control bus structures, avoiding a buffered set of signals and bridges between the buses.

The PCI Express connector and add-in card interfaces support the following auxiliary signals:

- ~~-~~REFCLK-/REFCLK+ (required): L~~l~~ow voltage differential signals. Requirements for REFCLK for a system are defined in *PCI Express Base Specification~~, Revision 4.0~~*. A system board must provide a reference clock that meets all requirements[1] for the common clock architecture defined for the reference clock in the *PCI Express Base Specification~~, Revision 4.0~~* and all the requirements defined in this specification.

  ~~**Note:** Requirements for REFCLK for a system are defined in *PCI Express Base Specification, Revision 4.0*. A system board must provide a reference clock that meets all requirements[2] for the common clock architecture defined for the reference clock in the *PCI Express Base Specification, Revision 4.0* and all the requirements defined in this specification.~~

- PERST# (required): I~~i~~ndicates when the applied main power is within the specified tolerance and stable. PERST# goes inactive after a delay of T_{PVPERL} time from the power rails achieving specified tolerance on power up.

- WAKE#: A~~a~~n open-drain, active low signal that is driven low by a PCI Express function to re-activate the PCI Express Link hierarchy's main power rails and reference clocks. It is required on any add-in card or system board that supports wakeup functionality compliant with this specification. WAKE# is also used by the system to signal to the PCI Express function in conjunction with the Optimized Buffer Flush/Fill (OBFF) mechanism.

- SMBCLK (optional): T~~t~~he SMBus interface clock signal. It is an open-drain signal.

- SMBDAT (optional): T~~t~~he SMBus interface address/data signal. It is an open-drain signal.

[1] The RMS jitter requirements are excluded. They are covered under the two port motherboard test methodology and requirements defined in this specification.

~~[2] The RMS jitter requirements are excluded. They are covered under the two port motherboard test methodology and requirements defined in this specification.~~

Formatted: Font: Garamond, 12 pt

Formatted: Font: 12 pt

Formatted: Font: Garamond, 12 pt

Formatted: Font: (Default) Garamond, 12 pt, Highlight

Formatted: Style Bullet box + Black, Don't suppress line numbers, Border: Top: (No border), Bottom: (No border), Pattern: Clear

Formatted: Font: (Default) Garamond, 12 pt

Formatted: Subscript

- JTAG (TRST#, TCLK, TDI, TDO, and TMS) (optional): T~~t~~he pins to support IEEE Standard 1149.1, Test Access Port and Boundary Scan Architecture (JTAG). They are included as an optional interface for PCI Express devices. IEEE Standard 1149.1 specifies the rules and permissions for designing an 1149.1-compliant IC.
- PRSNT1# (required): ~~a~~Add-in card presence detect pin. See Chapter 3 for a detailed description.
- PRSNT2# (required): ~~a~~Add-in card presence detect pin. See Chapter 3 for a detailed description.
- CLKREQ# (optional): The CLKREQ# signal is an open drain, active low signal that is driven low by the card to request that the PCI Express reference clock be available (active clock state) in order to allow the PCI Express interface to send/receive data. See the *PCI Express Mini-CEM Specification* for details on the functional and electrical requirements for the CLKREQ# signal. The CLKREQ# signal is also used by the optional L1 PM Substates mechanism. In this case, CLKREQ# can be asserted by either the system or add-in card to initiate an L1 exit. See the *PCI Express Base Specification~~, Revision 4.0~~* for details on the functional requirements for the CLKREQ# signal when implementing L1 PM Substates.

IMPLEMENTATION NOTE

CLKREQ# Processing on System Boards

To maintain backwards compatibility, system boards that support CLKREQ# must supply the reference clock to all add-in cards, regardless of the state of the CLKREQ# signal. Once the add-in card has been initialized and the system board is able to read the required configuration registers, the system can decide whether or not to allow the add-in card control the CLKREQ# signal.

- Add a implementation note that system boards must handle this correctly or add-in card may never get a clock.

- PWRBRK# (optional): ~~over power or over temperature condition. See Chapter 2 for a detailed description.~~A~~a~~n open-drain, active low signal that is driven low by the system to signal an Emergency Power Reduction ~~condition exists~~mechanism.

~~Note that t~~The SMBus interface pins are collectively optional for both the add-in card and the system board. If the optional management features are implemented, SMBCLK and SMBDAT are both required. Similarly, the JTAG pins are collectively optional. If this test mode is implemented, all the JTAG pins are required. For additional system requirements related to these signals refer to the *PCI Local Bus Specification~~, Revision 3.0~~*, ~~Section 4.3.3~~.

2.1. Reference Clock

2.1.1. Low Voltage Swing, Differential Clocks

To reduce jitter and allow for future silicon fabrication process changes, low voltage swing, differential clocks are being used, as illustrated in Figure 2-1~~Figure 2-1~~~~Figure 2-1~~. The nominal single-ended swing for each clock is 0 to 0.7 V and a nominal frequency of 100 MHz ±300 PPM. The clock has a defined crossover voltage range and monotonic edges through the input threshold regions as specified in Chapter 4.

Formatted: Indent: Left: 0", Hanging: 0.16"
Formatted: Font: Italic
Formatted: Font: Arial Black, 14 pt
Formatted: Font: 14 pt
Formatted: Font: Arial, 10 pt
Formatted: Body Text, Space Before: 3 pt, Border: Top: (Single solid line, Auto, 0.5 pt Line width, From text: 6 pt Border spacing:), Bottom: (Single solid line, 1.5 pt Line width, From text: 3 pt Border spacing:), Pattern: Clear (Gray-15%)
Formatted: Font: Arial, 10 pt, Bold
Formatted: Font: 10 pt
Formatted: Font: Arial, 10 pt, Bold
Formatted: Font: (Default) Arial, 10 pt
Formatted: Highlight
Formatted: Indent: Left: 0.13", No bullets or numbering
Commented [NM1]: Need a new implementation note?
Formatted: Highlight
Formatted: Not Highlight
Formatted: Font: Not Bold
Formatted: Font: Not Bold

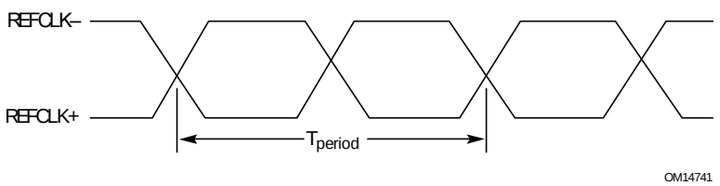


Figure 2-12-1: Differential REFCLK Waveform

The reference clock pair is routed point-to-point to each connector from the system board according to best-known clock routing rules. The reference clock distribution to all devices must be matched to within 15 inches on the system board. The transport delay delta between the data and clock at the Receiver is assumed to be less than 12 ns. The combination of the maximum reference clock mismatch and the maximum channel length will contribute approximately 9-10 ns and the remaining time is allocated to the difference in the insertion delays of the Tx and Rx devices. The routing of each signal in any given clock pair between the clock source and the connector must be well matched in length (< 0.005 inch) and appropriately spaced away from other non-clock signals to avoid excessive crosstalk.

~~The add-in card is required to use the reference clock on the connector. The add-in card is required to maintain the 600 ppm data rate matching specified in Section 4.3.7.1.1 of the *PCI Express Base Specification, Revision 3.0*.~~

Any terminations required by the clock are to be on the system board. An example termination topology for a current-mode clock generator is shown in Figure 2-2~~Figure 2-2~~~~Figure 2-2~~. EMI emissions will be reduced if clocks to open sockets are shut down at the clock source. The method for detecting the presence of a card in a slot and controlling the clock gating is platform specific and is not covered in this specification.

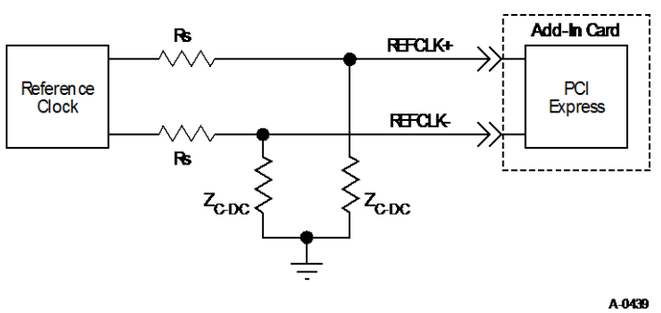


Figure 2-22-2: Example Current Mode Reference Clock Source Termination

Termination on the add-in card using discrete components on the PCB is not allowed~~, but~~ and is not covered by the specifications in Section 2.1.3. While the same measurement techniques can be used as specified in that section, Receiver termination will reduce the nominal swing and rise and fall times by half. The low input swing and low slew rates need to be validated against the clock Receiver requirements as they can cause excessive jitter in some clock input buffer designs.

The reference clock timings are based on nominal 100 Ω, differential pair routing with approximately 0.127 mm (5 mil) trace widths. This timing budget allows for a maximum add-in card trace length of 4.0 inches. No specific trace geometry, however, is explicitly defined in this specification.

2.1.2. Spread Spectrum Clocking (SSC)

The reference clocks may support spread spectrum clocking. Any given system design may or may not use this feature due to platform-level timing issues. The minimum clock period cannot be violated. The required method is to adjust the spread technique to not allow for modulation above the nominal frequency. This technique is often called "down-spreading." The requirements for spread spectrum modulation rate and magnitude are given in the *PCI Express Base Specification~~, Revision 4.0~~*.

Formatted: Body Text, Suppress line numbers

Formatted: Not Highlight

IMPLEMENTATION NOTE

Separate Ref-clock Independent SSC (SRIS) Considerations

Support of SRIS clocking via a standard CEM connector is allowed but represents a proprietary implementation and is not CEM compliant. The CEM form factor requires that the system board provide a common reference clock to all add-in cards connected to the system board via standard CEM compliant PCIe connectors. Similarly, add-in cards are required to use the provided common clock as the reference clock when communicating via a standard CEM compliant PCIe connector.

2.1.3. REFCLK AC Specifications

All specifications in Table 2-1~~Table 2-1~~~~Table 2-1~~ are to be measured using a test configuration as described in Note 11 with a circuit as shown in Figure 2-9~~Figure 2-9~~~~Figure 2-9~~.

Table 2-~~12-1~~: REFCLK DC Specifications and AC Timing Requirements

Symbol	Parameter	100 MHz Input		Unit	Note
		Min	Max		
Rising Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Falling Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150		mV	2
V_{IL}	Differential Input Low Voltage		-150	mV	2
V_{CROSS}	Absolute crossing point voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} over all rising clock edges		+140	mV	1, 4, 9
V_{RB}	Ring-back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is allowed	500		ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (including Jitter and Spread Spectrum modulation)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle jitter		150	ps	2
V_{MAX}	Absolute Max input voltage		+1.15	V	1, 7
V_{MIN}	Absolute Min input voltage		- 0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2
Rise-Fall Matching	Rising edge rate (REFCLK+) to falling edge rate (REFCLK-) matching		20	%	1,14
Z_{C-DC}	Clock source DC impedance	40	60	Ω	1, 11

Notes:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing. See Figure 2-7~~Figure 2-7~~~~Figure 2-7~~.
4. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 2-3~~Figure 2-3~~~~Figure 2-3~~.
5. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 2-3~~Figure 2-3~~~~Figure 2-3~~.
6. Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative PPM tolerance, and spread spectrum modulation. See Figure 2-6~~Figure 2-6~~~~Figure 2-6~~.

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt

7. Defined as the maximum instantaneous voltage including overshoot. See ~~Figure 2-3~~Figure 2-3~~Figure 2-3~~.
8. Defined as the minimum instantaneous voltage including undershoot. See ~~Figure 2-3~~Figure 2-3~~Figure 2-3~~.
9. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system. See ~~Figure 2-4~~Figure 2-4~~Figure 2-4~~.
10. Refer to ~~Section 4.3.7.1.1~~Chapter 9 of the *PCI Express Base Specification*, ~~*Revision 4.0*~~ for information regarding PPM considerations.
11. System board compliance measurements must use the test load card described in ~~Figure 2-9~~Figure 2-9~~Figure 2-9~~. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2 pF.
12. T_{STABLE} is the time the differential clock must maintain a minimum ±150 mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100 mV differential range. See ~~Figure 2-8~~Figure 2-8~~Figure 2-8~~.
13. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000 MHz exactly or 100 Hz. For 300 PPM, then we have an error budget of 100 Hz/PPM * 300 PPM = 30 kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±300 PPM applies to systems that do not employ Spread Spectrum Clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500 PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,800 PPM.
14. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See ~~Figure 2-5~~Figure 2-5~~Figure 2-5~~.

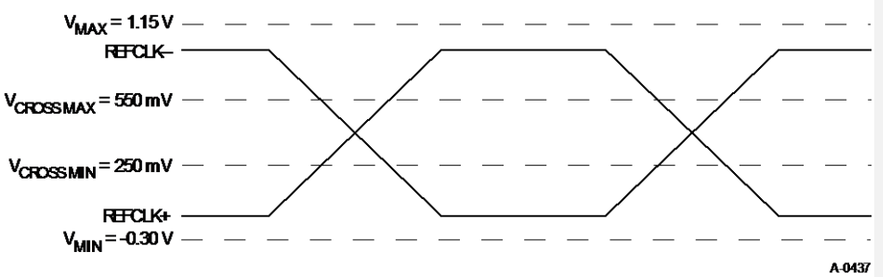


Figure 2-~~3~~2 ~~3~~: Single-Ended Measurement Points for Absolute Cross Point and Swing

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt

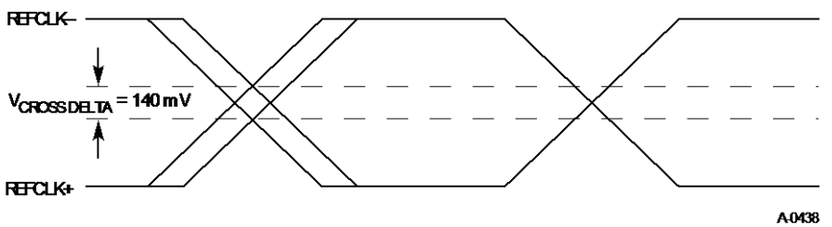


Figure 2-42-4: Single-Ended Measurement Points for Delta Cross Point

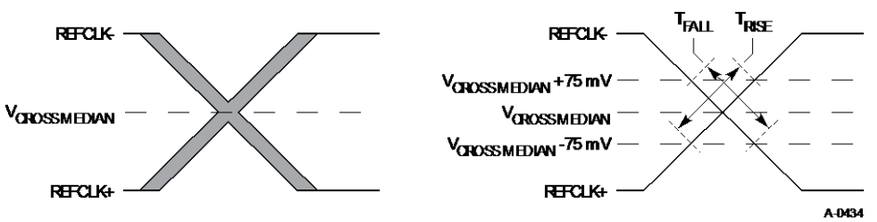


Figure 2-52-5: Single-Ended Measurement Points for Rise and Fall Time Matching

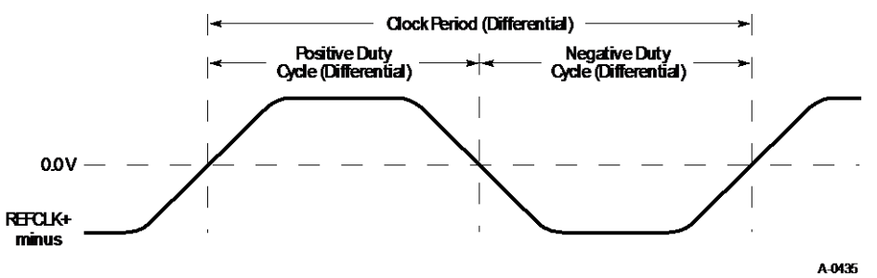


Figure 2-62-6: Differential Measurement Points for Duty Cycle and Period

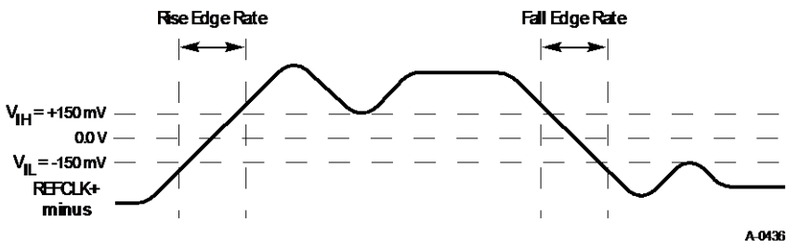


Figure 2-~~72-7~~: Differential Measurement Points for Rise and Fall Time

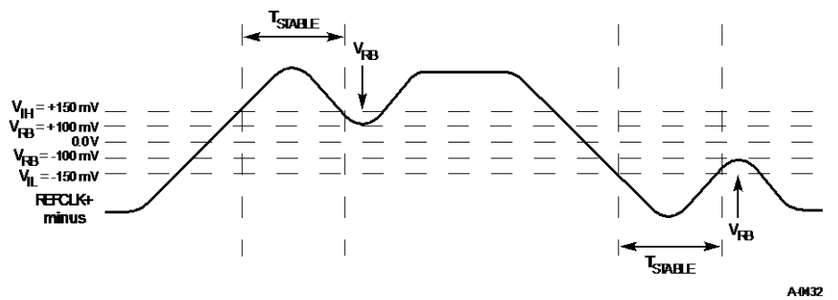


Figure 2-~~82-8~~: Differential Measurement Points for Ringback

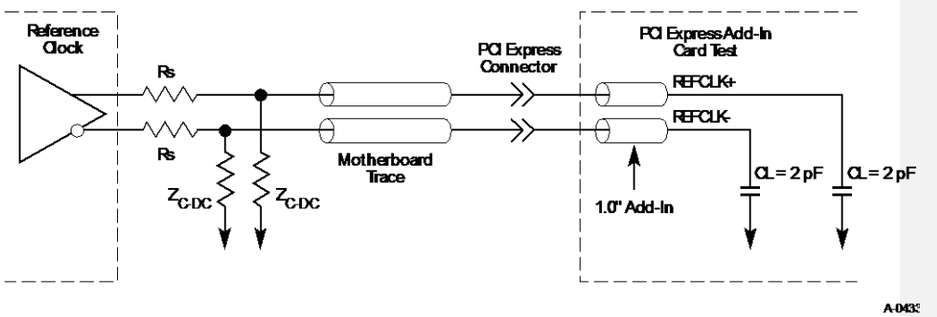


Figure 2-~~92-9~~: Reference Clock System Measurement Point and Loading

2.1.4. REFCLK Phase Jitter Specification for 2.5 GT/s, 5.0 GT/s, 8.0 GT/s and 16.0GT/s Signaling Support

The phase jitter specification and measurement methodology is discussed in Chapter 9~~Section TBD~~ of the *PCI Express Base Specification* ~~r4.0~~.

Formatted: Font: Italic

To account for phase jitter on the REFCLK, a two port methodology for simultaneously assessing the system board data and reference clock is described with specified limits in the appropriate sections below.

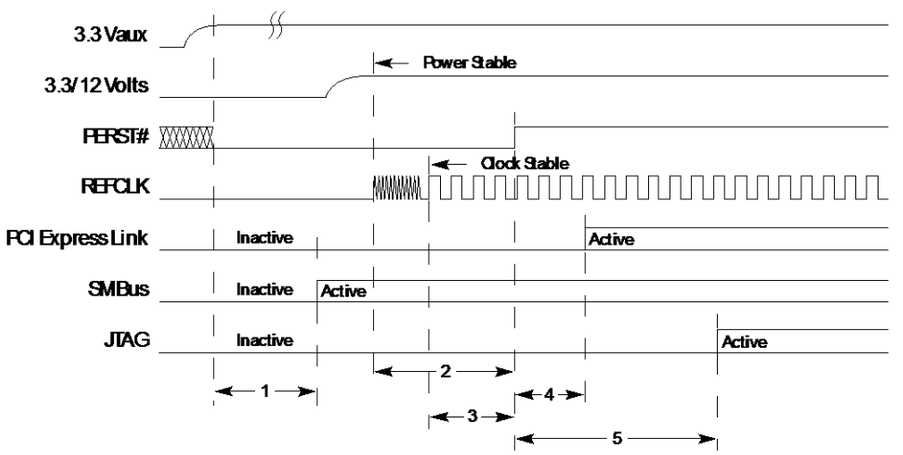
2.2. PERST# Signal

The PERST# signal is used to indicate when the power supply is within its specified voltage tolerance and is stable. It also initializes a component's state machines and other logic once power supplies stabilize. On power up, the deassertion of PERST# is delayed 100 ms (T_{PVPERL}) from the power rails achieving specified operating limits. Also, within this time, the reference clocks (REFCLK+, REFCLK-) also become stable, at least $T_{PERST-CLK}$ before PERST# is deasserted. PERST# is asserted in advance of the power being switched off in a power-managed state like S3. PERST# is asserted when the power supply is powered down, but without the advanced warning of the transition.

2.2.1. Initial Power-Up (G3 to S0)

As long as PERST# is active, all PCI Express functions are held in reset. The main supplies ramp up to their specified levels (+3.3-V and +12-V). Some time during this stabilization time, the REFCLK starts and stabilizes. After there has been time (T_{PVPERL}) for the power and clock to become stable, PERST# is deasserted high and the PCI Express functions can start up.

On initial power-up, the hardware default state of the Active State Power Management Control field in the Link Control register must be set to 00b. The state of this field may be changed by the system BIOS or the operating system. Other software agents should not change this field.



1. 3.3Vaux stable to SMBus driven (optional). If no 3.3Vaux on platform, the delay is from +3.3V stable
2. Minimum time from power rails within specified tolerance to PERST# inactive (T_{PVPERL})
3. Minimum clock valid to PERST# inactive ($T_{PERST-CLK}$)
4. Minimum PERST# inactive to PCI Express link out of electrical idle
5. Minimum PERST# inactive to JTAG driven (optional)

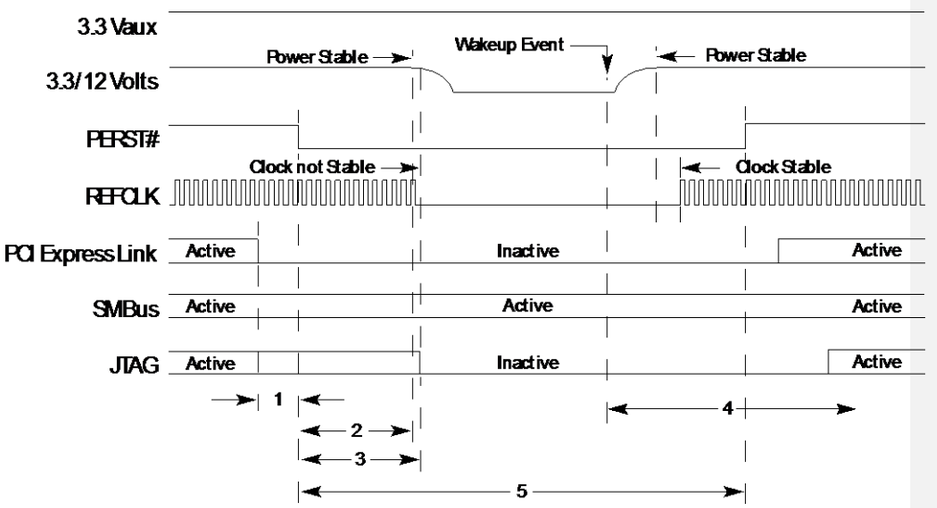
OM14742B

Figure 2-~~10~~2-~~10~~: Power Up

2.2.2. Power Management States (S0 to S3/S4 to S0)

If the system wants to enter S3/S4, devices are placed into $D3_{hot}$ states with Links in L2 prior to any power transitions at the slot. The main power and reference clock supplied to the PCI Express slot will go inactive and stay inactive until a wakeup event. As a result of the removal of main power, devices enter the $D3_{cold}$ state. During the $D3_{cold}$ state, +3.3Vaux remains at +3.3-V. On the wakeup event, the power manager restores the main power and reference clocks. As in the last section, PERST# deasserts T_{PVPERL} after the clock and power are stable.

On resume from a $D3_{cold}$ state, the hardware default state of the Active State Power Management Control field in the Link Control register must be set to 00b. The state of this field may be changed by the system BIOS or the operating system. Other software agents should notchange this field.



1. The PCI Express link will be put into electrical idle prior to PERST# going active.
2. PERST# goes active before the power on the connector is removed.
3. Clock and JTAG go inactive after PERST# goes active.
4. A wakeup event resumes the power to the connector, restarts the clock, and the sequence proceeds as in power up.
5. The minimum active time for PERST# is T_{PERST}.

OM14743

Figure 2-~~11~~12-~~11~~: Power Management States

2.2.3. Power Down

A power rail (+12-V, +3.3-V, or +3.3Vaux) is deemed to be valid or stable if the specified voltage is within the associated voltage tolerances defined in Table 4-1~~Table 4-1~~~~Table 4-1~~. Once a power rail is deemed stable, an invalid or unstable rail is defined as a rail that has dropped below the specified minimum voltage levels (e.g., below +3.00 V for the +3.3-V rails). For purposes of detecting an out-of-tolerance power source, the threshold for detection should be established in a window range of no more than 500 mV below the specified minimum voltage level for the +3.3-V and +3.3Vaux rails (i.e., +2.50 V) and +1.34 V below for the +12-V rail (i.e., +9.70 V). Figure 2-12~~Figure 2-12~~~~Figure 2-12~~ illustrates these threshold windows.

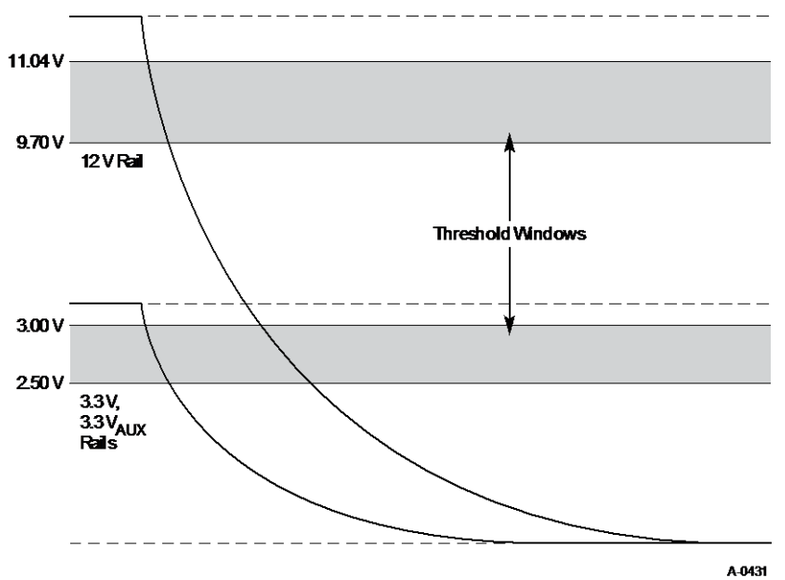
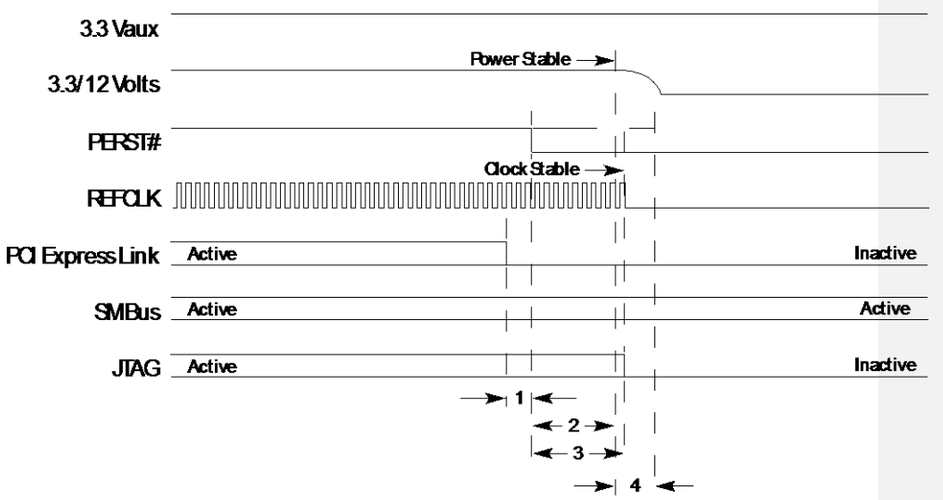


Figure 2-12~~2-12~~: Out-of-tolerance Threshold Windows



1. The PCI Express link will be put into an inactive state (Device in $D3_{hot}$) prior to PERST# going active, except in the case of a surprise power down.
2. PERST# goes active before the power on the connector is removed.
3. Clock and JTAG go inactive after PERST# goes active.
4. In the case of a surprise power down, PERST# goes active T_{FAIL} after power is no longer stable.

OM14744

Figure 2-~~13~~2-~~13~~: Power Down

2.3. WAKE# Signal

The WAKE# signal is an open drain, active low signal that is driven low by a PCI Express component to reactivate the PCI Express slot's main power rails and reference clocks. The WAKE# signal is also used by Downstream Ports to signal to functions on the add-in card in conjunction with the OBFF mechanism. Only add-in cards that support either the wake process or the OBFF mechanism connect to this pin. If the add-in card has wakeup capabilities, it must support the WAKE# function. Likewise, only systems that support the wakeup function or the OBFF mechanism need to connect to this pin. Such systems are not required to support Beacon as a wakeup mechanism, but are encouraged to support it. If the wakeup process is used, the +3.3Vaux supply must be present and used for this function. The assertion and de-assertion of WAKE# are asynchronous to any system clock. (See Chapter 5 of the *PCI Express Base Specification, ~~Revision 4.0~~* for more details on PCI-compatible power management.)

If the WAKE# signal is supported by a slot, the signal is connected to the platform's power management (PM) controller. WAKE# may be bused to multiple PCI Express add-in card connectors, forming a single input connection at the PM controller, or individual connectors can have individual connections to the PM controller. Hot-Plug requires that WAKE# be isolated between connectors and driven inactive during the Hot-Plug/Hot Removal events. Refer to Section 6.1 for the connector pin assignment for the WAKE# signal.

Auxiliary power (+3.3Vaux) must be used by the asserting and receiving ends of WAKE# in order to revive the hierarchy. The system vendor must also provide a pull-up on WAKE# with its bias voltage reference being supplied by the auxiliary power source in support of Link reactivation. ~~Note that t~~The voltage that the system board uses to terminate the WAKE# signal can be lower than the auxiliary supply voltage to be compatible with lower voltage processes of the system PM controller. However, all potential drivers of the WAKE# signal must be +3.3 V tolerant.

WAKE# must only be asserted by the add-in card when all of its functions are in the D3 state and at least one of its functions is enabled for wakeup generation using the PME Enable bit in the PMCSR.

~~Note:~~ WAKE# is not PME# and should not be attached to the PCI-PME# interrupt signals. WAKE# causes power to be restored but must not directly cause an interrupt.

If the PCI Express add-in card supports the OBFF mechanism defined in the *PCI Express Base Specification*, then the WAKE# signal may be used as an input to the add-in card. Refer to Chapter 6 ~~Section 6.19~~ of the *PCI Express Base Specification* for specifics of the OBFF mechanism.

Formatted: Not Highlight

Formatted: Not Highlight

WAKE# has additional electrical requirements over and above standard open drain signals that allow it to be shared between devices that are powered off and those that are powered on using auxiliary power for example. The additional requirements include careful circuit design to ensure that a voltage applied to the WAKE# signal network never causes damage to a component even if that particular component's power is not applied.

Additionally, the device must ensure that it does not pull WAKE# low unless WAKE# is being intentionally asserted in all cases, including when the related function is in $D3_{cold}$.

This means that any component implementing WAKE# must be designed such that:

- Unpowered WAKE# output circuits are not damaged if a voltage is applied to them from other powered "wire-ORed" sources of WAKE#.
- When power is removed from its WAKE# generation logic, the unpowered output does not present a low impedance path to ground or any other voltage.

These additional requirements ensure that the WAKE# signal network continues to function properly when a mixture of auxiliary powered and unpowered components have their WAKE# outputs wire-ORed together. ~~It is important to note~~Be aware that most commonly available open drain and tri-state buffer circuit designs used "as is" do not satisfy the additional circuit design requirements for WAKE#.

Other requirements on the system board/add-in card designer include:

- Common ground plane reference between slots/components attached to the same WAKE# signal.
- Split voltage power planes (+3.3Vaux vs. +3.3V) are required if +3.3Vaux is supplied to the connector(s).
- If +3.3Vaux is supplied to one PCI Express connector in a chassis, it must be supplied to all PCI Express connectors in that chassis.
- If WAKE# is supported on one PCI Express connector in a chassis, it must be supported on all PCI Express connectors in that chassis.
- If the system does not support +3.3Vaux or the wakeup function, the +3.3Vaux connector pin is left open on the system board. See the *PCI Bus Power Management Interface Specification*, ~~Revision 1.2~~ for +3.3Vaux power requirements.
- +3.3Vaux voltage supply may be present even if the device is not enabled for wakeup events.
- +3.3-V at the PCI Express connector may be switched off by the system.
- Add-in cards are permitted to generate the Beacon wakeup mechanism in addition to using the WAKE# mechanism, although the system is not required to provide support for Beacon.
- ~~Note:~~ If the add-in card uses the Beacon mechanism in addition to the WAKE# mechanism, the Beacon may be ignored by the system. Circuits that support the wake function and are intended to work in any PCI Express system must be designed to generate the Beacon on their PCI Express data lines.

PCI Express add-in card designers must be aware of the special requirements that constrain WAKE# and ensure that their add-in cards do not interfere with the proper operation of the WAKE# network. The WAKE# input into the system may de-assert as late as 100 ns after the WAKE# output from the function de-asserts (i.e., the WAKE# pin must be considered indeterminate for a number of cycles after it has been de-asserted).

The value of the pull-up resistor for WAKE# on the system board must be derived taking into account the total possible capacitance on WAKE# to ensure that WAKE# charges up to a logic high voltage level in no more than 100 ns. (See Chapter 4~~Section 4.3.3~~ of the *PCI Local Bus Specification, ~~Revision 3.0~~* for information on pull-up resistors.)

Formatted: Font: Italic

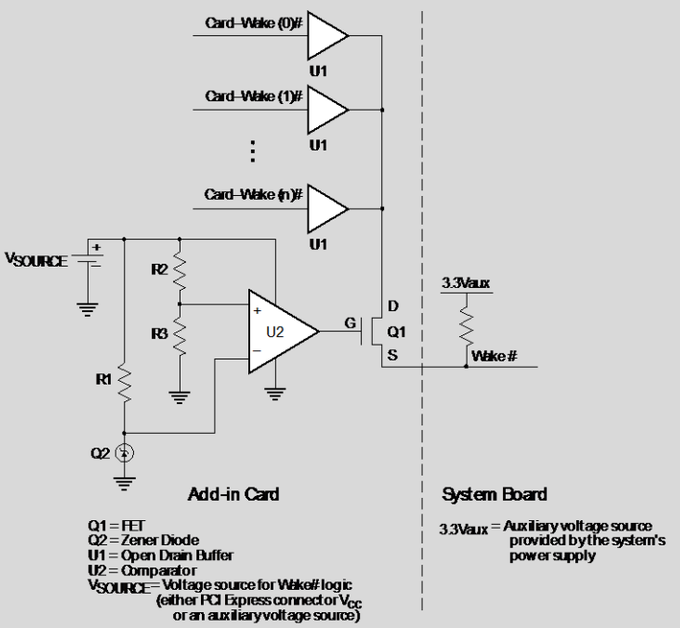
IMPLEMENTATION NOTE

Example WAKE# Circuit Design

The following diagram is an example of how the WAKE# generation logic could be implemented. In this example, multiple PCI Express functions have their WAKE# signals ganged together and connected to the single WAKE# pin on the PCI Express add-in card connector.

The circuit driving the gate of transistor Q1 is designed to isolate the add-in card's WAKE# network from that of the system board whenever its power source (V_{SOURCE}) is absent.

If the card supplies power to its WAKE# logic with the PCI Express connector's +3.3-V supply (i.e., it does not support wakeup from $D3_{cold}$), then all WAKE# sources from the card will be isolated from the system board when the add-in card's +3.3-V rail is switched off. Add-in cards that support wakeup from $D3_{cold}$ have an auxiliary power source (+3.3Vaux) to power the WAKE# logic which maintains connection of these WAKE# sources to the system board's WAKE# signal network even when the Link hierarchy's power (+3.3-V) has been switched off.



This example assumes that all sources of WAKE# on the add-in card are powered by either the +3.3-V or +3.3Vaux (VSOURCE). If WAKE# from D3cold is supported by some, but not all of the add-in card's functions that generate WAKE#, the add-in card designer must ensure that there is separate isolation control for each of the WAKE# generation power sources.

PCI Express component designers could choose to integrate the "power fail detect" isolation circuitry with their WAKE# output pin physically corresponding to the source of FET Q1. Alternatively, all isolation control logic could be implemented externally on the add-in card.

Formatted: Right: 0"

This example is meant as a conceptual aid, and is not intended to prescribe an actual implementation.

2.4. SMBus (Optional)

The optional System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate with each other and with the rest of the system. It is based on the principles of operation of I^2C.

SMBus provides a control bus for system and power management related tasks. A system may use SMBus to pass messages to and from devices instead of tripping individual control lines. Removing the individual control lines reduces pin count. Accepting messages ensures future expandability.

With SMBus, a device can provide manufacturer information, tell the system what its model/part number is, save its state for a suspend event, report different types of errors, accept control parameters, and return its status.

SMBus is described in *System Management Bus (SMBus) Specification~~, Version 2.0~~*. Refer to this specification for DC characteristics and all AC timings. If the system board or add-in card supports SMBus, it must adhere to additional requirements that may be found in Chapter 8 of the *PCI Local Bus Specification~~, Revision. 3.0~~*.

The system board provides pull-ups to the +3.3Vaux rail per the above specification and the components attached to these signals need to have a +3.3 V signaling tolerance.

2.4.1. Capacitive Load of High-power SMBus Lines

Capacitive load for each bus line includes all pin, wire, and connector capacitances. The maximum capacitive load affects the selection of the pull-up resistor or the current source in order to meet the rise time specifications of SMBus.

Normally, pin capacitance is defined as the total capacitive load of one SMBus device as seen in a typical manufacturer's data sheet. The value in the DC specifications (C_{OUT} in Table 2-2~~Table 2-2Table 2-3~~) is a recommended guideline so that two SMBus devices may, for example, be populated on an add-in card.

2.4.2. Minimum Current Sinking Requirements for SMBus Devices

While SMBus devices used in low-power segments have practically no minimum current sinking requirements due to the low pull-up current specified for low-power segments, devices in high-power segments are required to sink a minimum current of 4 mA while maintaining the V_{OL}(max) of 0.4 V. The requirement for 4 mA sink current determines the minimum value of the pull-up resistor R_P that can be used in SMBus systems.

2.4.3. SMBus "Back Powering" Considerations

Unpowered devices connected to either a low-power or high-power SMBus segment must provide, either within the device or through the interface circuitry, protection against "back powering" the

SMBus. Unpowered devices connected to high-power segments must meet leakage specifications in ~~Section 3.1.2.1~~Chapter 3 of the *System Management Bus (SMBus) Specification~~, Version 2.0~~*.

2.4.4. Power-on Reset

SMBus devices detect a power-on event in one of three ways:

By detecting that power is being applied to the device

By PERST# being asserted

For self-powered or always powered devices, by detecting that the SMBus is active (clock and data lines have gone high after being low for more than 2.5 s)

A~~n~~ SMBus device must respond to a power-on event by bringing the device into an operational state within t_{POR}, defined in ~~Table~~ Layer 1 of the *System Management Bus (SMBus) Specification~~, Version 2.0~~*, after the device has been supplied power that is within the device's normal operating range. Self-powered or always-powered devices, such as Smart Batteries, are not required to do a complete power-on reset, but they must be in an operational state within 500 ms after the SMBus becomes active.

2.5. JTAG Pins (Optional)

The *IEEE Standard 1149.1, Test Access Port and Boundary Scan Architecture*, is included as an optional interface for PCI Express devices. *IEEE Standard 1149.1* specifies the rules and permissions for designing an 1149.1-compliant interface. Inclusion of a Test Access Port (TAP) on an add-in card allows boundary scan to be used for testing of the card on which it is installed. The TAP is comprised of four pins (optionally five) that are used to interface serially with a TAP controller within the PCI Express device.

TCK	in	*Test Clock* is used to clock state information and test data into and out of the device during operation of the TAP.
TDI	in	*Test Data Input* is used to serially shift test data and test instructions into the device during TAP operation.
TDO	out	*Test Output* is used to serially shift test data and test instructions out of the device during TAP operation.
TMS	in	*Test Mode Select* is used to control the state of the TAP controller in the device.
TRST#	in	*Test Reset* provides an asynchronous initialization of the TAP controller. This signal is optional in *IEEE Standard 1149.1*.

These TAP pins operate at +3.3 V, the same as the other single-ended I/O signals of the PCI Express connector. The drive strength of the TDO pin is not required to be the same as other PCI Express pins. The add-in card vendor must specify TDO drive strength. The direction of these TAP pins is defined from the perspective of the add-in card.

The system vendor is responsible for the design and operation of the 1149.1 serial chains ("rings") required in the system. The signals are supplementary to the PCI Express interface. Additional information can be found in the *PCI Local Bus Specification, ~~Revision 3.0~~,* ~~Section 2.2.9~~Chapter 2.

2.6. PWRBRK# Signal (Optional)

~~TBD: PWRBRK ECN needs to be submittend in order to fill in this section.~~ The PWRBRK# signal is an optional normative capability applicable to the CEM form factor. Only add-in cards that support Emergency Power Reduction connect to this pin. Likewise, only systems that support the Emergency Power Reduction mechanism connect to this pin. The assertion and de-assertion of PWRBRK# are asynchronous to any system clock. An add-in card that supports Emergency Power Reduction must provide a weak pull-up on PWRBRK# (minimum 95KΩ). A system that supports Emergency Power Reduction must provide a stronger pull-up on PWRBRK#. These pull-up resistor values must ensure meeting the rise time specification of T_{PWRBRK}.

The PWRBRK# signal is used to communicate requests to enter and exit the Emergency Power Reduction State. See *PCI Express Base Specification*, ~~Section 6.x.~~*Chapter 6*

PWRBRK# is an open-drain, active low signal that is driven low by an external enclosure component. When asserted, add-in card that support Emergency Power Reduction must quickly reduce their power consumption. When de-asserted, add-in cards that support Emergency Power Reduction are permitted to resume normal power consumption. The add-in card should debounce this input to avoid thrashing the system with rapid transitions in and out of the Emergency Power Reduction State.

This mechanism is an emergency fail-safe intended to be used to prevent system damage and is not intended to provide normal dynamic power management. The external enclosure should control how it asserts / deasserts this signal to avoid thrashing the system with rapid transitions in and out of the Emergency Power Reduction State. The amount of power consumed in the Emergency Power Reduction state is communicated through the Power Budgeting extended capability as defined in the *PCI Express Base Specification* (see ~~Section 7.15~~)Chapter 7). The time allowed to achieve this power reduction ($T_{PWRBRK-AIC-ENTER-LP-MODE}$) is defined in Table 2-3~~Table 2-3~~.

Add-in cards that support Emergency Power Reduction may contain any mix of Devices that advertise support for PWRBRK# or that don't advertise such support. Software is not required to configure or enable use of PWRBRK#. Software can optionally use the mechanisms defined in the PCI Express Base Specification to determine support for PWRBRK# and, if supported, to determine the associated power saving. Software can detect that a supporting Function has entered the Emergency Power Reduction State.

Electrical specifications for PWRBRK# at the CEM connector are defined in Table 2-2~~Table 2-2~~. Timing requirements are defined in Table 2-3~~Table 2-3~~ and ~~-~~Figure 2-15.

PWRBRK# may be bused to multiple PCI Express add-in card connectors, forming a single output connection at the external enclosure component, or individual connectors can have individual connections to the external enclosure component.

Formatted: Subscript

Formatted: Font: Italic, Highlight

Formatted: Font: Italic

Formatted: Font: Italic

Formatted: Font: Italic

Formatted: Subscript

2.7. Auxiliary Signal Parametric Specifications

2.7.1. DC Specifications

Table 2-~~22~~ ~~3~~: Auxiliary Signal DC Specifications - PERST#, WAKE#, CLKREQ#, SMBus and PWRBRK#

Symbol	Parameter	Conditions	Min	Max	Unit	Notes
V_{IL1}	Input Low Voltage		-0.5	+0.8	V	2, 6, 7
V_{IH1}	Input High Voltage		+2.0	V_{cc3_3}~~+3.3V~~ + 0.5	V	2, 6, 7
V_{IL2}	Input Low Voltage		-0.5	+0.8	V	4
V_{IH2}	Input High Voltage		+2.1	~~V_{ccSus3_3}~~+3.3Vaux + 0.5	V	4
V_{OL1}	Output Low Voltage	4.0 mA		+0.2	V	1, 3
V_{HMAX}	Max High Voltage			V_{cc3_3}~~+3.3V~~ + 0.5	V	3
V_{OL2}	Output Low Voltage	4.0 mA		+0.4	V	1, 4
I_{in}	Input Leakage Current	0 to +3.3 V	-10	+10	µA	2, 4, 7
I_{lkg}	Output Leakage Current	0 to +3.3 V	-50	+50	µA	3, 5
C_{in}	Input Pin Capacitance			7	pF	2, 7
C_{out}	Output (I/O) Pin Capacitance			30	pF	3, 4

Notes:

1. Open-drain output a pull-up is required on the system board. There is no V_{OH} specification for these signals. The number given is the maximum voltage that can be applied to this pin.
2. Applies to PERST#.
3. Applies to WAKE#.
4. Applies to SMBus signals SMBDATA and SMBCLK.
5. Leakage at the pin when the output is not active (high impedance).
6. Applies to WAKE# issued by Switch Downstream Ports and Root Complex for signaling of OBFF indications as received at the input of the Endpoint(s).
7. ~~6.~~ Applies to PWRBRK#.

2.7.2. AC Specifications

Table 2-~~3~~2 ~~4~~4: Power Sequencing and Reset Signal Timings

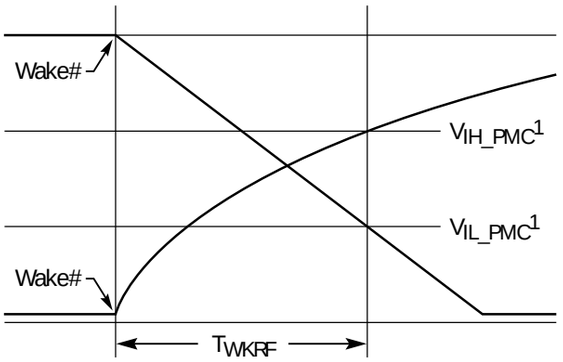
Symbol	Parameter	Min	Max	Units	Notes	Figure
T_{PVPERL}	Power stable to PERST# inactive	100		ms	1	Figure 2-10~~Figure 2-10~~Figure 2-10
$T_{PERST-CLK}$	REFCLK stable before PERST# inactive	100		µs	2	Figure 2-10~~Figure 2-10~~Figure 2-10
T_{PERST}	PERST# active time	100		µs		Figure 2-11~~Figure 2-11~~Figure 2-11
T_{FAIL}	Power level invalid to PERST# active		500	ns	3	Figure 2-13~~Figure 2-13~~Figure 2-13
T_{WKRF}	WAKE# rise – fall time		100	ns	4	Figure 2-14~~Figure 2-14~~Figure 2-14
$T_{WAKE-TX-MIN-PULSE}$	Minimum WAKE# pulse width;applies to both active-inactive-active and inactive-active-inactive cases	300		ns	5	
$T_{WAKE-FALL-FALL-CPU-ACTIVE}$	Time between two falling WAKE# edges when signaling CPU Active	700	1000	ns	5	
$T_{PWRBRKRF}$	PWRBRK# rise – fall time		100	ns	6	
$T_{PWRBRK-FALL-RISE-ACTIVE}$	Time PWRBRK# is active	1		ms	6	
$T_{PWRBRK-RISE-FALL-INACTIVE}$	Time PWRBRK# is inactive	1		ms	6	
$T_{PWRBRK-AIC-ENTER-LP-MODE}$	Time for Add-in card to enter low power mode		10	µs		

Notes:
1. Any supplied power is stable when it meets the requirements specified for that power supply.
2. A supplied reference clock is stable when it meets the requirements specified for the reference clock. The PERST# signal is asserted and de-asserted asynchronously with respect to the supplied reference clock.
3. The PERST# signal must be asserted within T_{FAIL} of any supplied power going out of specification.
4. Measured from WAKE# assertion/de-assertion to valid input level at the system PM controller. Since WAKE# is an open-drain signal, the rise time is dependent on the total capacitance on the platform and the system board pull-up resistor. It is the responsibility of the system designer to meet the rise time specification.
5. Refers to timing requirement for indicating an active window.

Formatted Table

Formatted: Subscript, Small caps

~~5.~~6. Refers to PWRBRK# timing diagram in Figure 2-15.



Note 1: Power Management Controller input switching levels are platform dependent and are not set by this specification.

A-0338

Figure 2-~~14~~2-14: WAKE# Rise and Fall Time Measurement Points

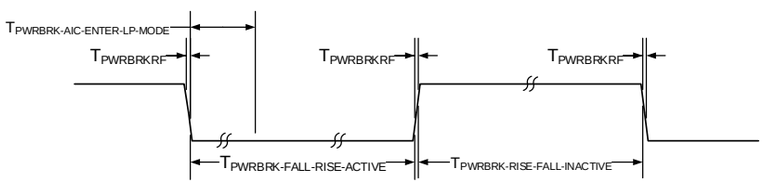


Figure 2-15: PWRBRK# Timing Requirement Diagram

~~**Figure 2-15: PWRBRK# Timing Requirement Diagram**~~

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Font color: Black

3

3. Hot Insertion and Removal

In the following text, all references to mechanical elements should be interpreted in the context of the PCI Express card form factor definition, unless otherwise stated.

3.1. Scope

The PCI Express specification natively supports Hot-Plug/Hot Removal of PCI Express add-in cards. However, hardware support of Hot-Plug/Hot-Removal on the system board is optional. Since the PCI Express evolutionary form factor is designed as a direct PCI connector replacement and utilizes an edge card connector, the PCI Express Native Hot-Plug model is based on the standard usage model defined in the *PCI Standard Hot-Plug Controller and Subsystem Specification~~, Revision 1.0~~*.

Section 3.2 describes the add-in card presence detect and PCI Express Native Hot-Plug signals. For a detailed explanation of the register requirements and standard usage model, see Chapter 7 of the *PCI Express Base Specification~~, Revision 4.0~~*.

3.2. Presence Detect

The PCI Express Hot-Plug controller detects the presence of an add-in card using the PRSNT2# signal as shown in Figure 3-1~~Figure 3-1~~Figure 3-1. It is the responsibility of the ~~Root Complex or the Switch~~Downstream Port to determine the presence of the add-in card and set the ~~present~~ presence detected bits in the appropriate register as described in Chapter 7 of the *PCI Express Base Specification~~, Revision 4.0~~*. In addition to the Hot-Plug controller, the PRSNT2# signal is used by the system board to recognize the presence of the add-in card in order to enable the auxiliary signals: REFCLK, PERST#, SMBus group, and JTAG group. The two signals, PRSNT1# and PRSNT2#, described in Figure 3-1~~Figure 3-1~~Figure 3-1, are required on the PCI Express connector and must be supported by all PCI Express add-in cards.

Both PRSNT1# and PRSNT2# signals are required in order to detect the presence of the add-in card and to ensure that it is fully inserted in the connector. ~~Note that t~~The pads on the add-in card for the PRSNT1# and PRSNT2# signals are shorter than the rest of the pads in order to have about 1 ms difference of insertion time. Unused PRSNT2# pads on x4, x8, and x16 add-in cards can be either standard length or ~~the pad can be eliminated~~shorter. This scheme is used to allow the power switches to isolate the power to the card during surprise removal. The mechanical details are provided in Chapter 6.

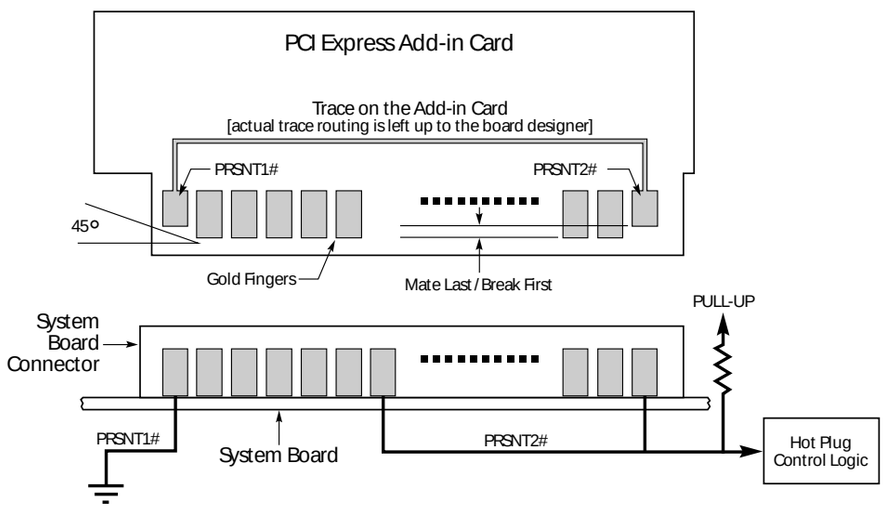


Figure 3-~~1~~3-1: Presence Detect in a Hot-Plug Environment

It is required that all PCI Express add-in cards implement variable-length edge ~~-~~finger pads and tie the PRSNT1# and PRSNT2# signals together on the add-in card. There is more than one PRSNT2# pin defined in the x4, x8, and x16 PCI Express connectors; these are needed to support up-plugging. All add-in cards shall connect the PRSNT1# signal to the farthest-apart PRSNT2# signal with a single trace in between them as illustrated in Figure 3-1~~Figure 3-1~~Figure 3-1. For example, a x4 add-in card would connect PRSNT1# with PRSNT2# on pin B31, and a x8 add-in card would connect PRSNT1# with PRSNT2# on pin B48. Refer to Table 6-1~~Table 6-1~~Table 6-1 for connector pin numbering and definition. If the system board designer chooses to implement hot-plug support, the system board must connect PRSNT1# to GND and separately connect all the PRSNT2# pins together to a single pull-up resistor, as shown in Figure 3-1~~Figure 3-1~~Figure 3-1. The system board designer determines the pull-up resistor voltage and associated use of applicable hot-plug control logic. If the system board designer chooses not to implement hot-plug support, PRSNT1# and PRSNT2# connector pins may either be left unconnected or may be grounded on the system board.

Since the x8 add-in card may plug into a x8 connector with a x4 Link only, the system board shall have the two PRSNT2# pins (B31 and B48) connected together. This is required in order to sense the presence of the x8 add-in card in a x8 connector that supports a x4 Link only. See Section 9.~~5~~9.~~5~~9.3 for card interoperability discussions.

4

4. Electrical Requirements

Power delivery requirements defined in this chapter apply not only to add-in cards, but also to connectors and systems.

4.1. Power Supply Requirements

All PCI Express add-in card connectors require two power rails: +12-V and ~~+3.3 V~~3.3V, with a third, optional +3.3Vaux rail. Systems that provide PCI Express add-in card connectors are required to provide both the +12-V and +3.3-V rails to every PCI Express add-in card connector in the system. The +3.3Vaux rail may be supplied to the PCI Express add-in card connectors at the system board designers' discretion. However, if a system board designer does supply +3.3Vaux to the PCI Express add-in card connector, the +3.3Vaux rail must be supplied to all PCI Express add-in card connectors. In addition, as described in Chapter 2, if the platform with the PCI Express interface supports the WAKE# signal, the +3.3Vaux rail (as well as the WAKE# signal) must be supplied to all PCI Express add-in card connectors.

~~A system that supports a PCI Express 150 W-ATX add-in card can deliver the +12 V to the standard connector and the additional +12 V via the dedicated power supply connector from the same or different rails in the power supply. This is up to the discretion of the system designer.~~

Table 4-1~~Table 4-1~~~~Table 4-1~~ provides the required specifications for the power supply rails available at the PCI Express slots and ~~the 150 W-ATX~~any auxiliary power connectors. The system designer is responsible for ensuring that the power delivered to the PCI Express connectors meets the specifications called out in Table 4-1~~Table 4-1~~~~Table 4-1~~.

An effort is currently underway to refine the power management capabilities described below. Specifically, additional support for power levels greater than 300 W including finer granularity of power utilization, e.g. 5 W steps, is being considered. Also a mechanism of specifying and measuring dynamic power utilization is being developed. This work will be included in the next revision of this specification.

Table 4-14-1: Power Supply Rail Requirements

Power Rail	10-10 W Slot	25-25 W Slot	75 W Slot	150W-ATX 2-x x 3 or 2 x 4 Auxiliary Power Connector	2 x 4 Auxiliary Power Connector
+3.3-V (Vcc3_3)					
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)	N/A	N/A
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)		
Capacitive Load	1000 µF (max)	1000 µF (max)	1000 µF (max)		
+12-V					
Voltage tolerance	± 8%	± 8%	± 8%	+5% / -8% (max)	+5% / -8% (max)
Supply Current	0.5 A (max)	2.1 A (max)	5.5 A (max)		
Capacitive Load	300 µF (max)	1000 µF (max)	2000 µF (max)	6.25-25 A (max)	12.5 A (max)
+3.3Vaux					
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)	N/A	N/A
Supply Current					
Wakeup Enabled	375 mA (max)	375 mA (max)	375 mA (max)		
Non-wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)		
Capacitive Load	150 µF (max)	150 µF (max)	150 µF (max)		

Notes:

1. The maximum current slew rate for each add-in card shall be no more than 0.1 A/µs.
2. Each add-in card shall limit its bulk capacitance on each power rail to less than the values shown in Table 4-1Table 4-1Table 4-1.
3. System boards that support Hot-Plug add-in cards shall limit the voltage slew rate so that the inrush current to the card shall not exceed the specified maximum current. This is calculated by the equation dV/dt = I/C; where:
   I = maximum allowed current (A)
   C = maximum allowed bulk capacitance (F)
   dV/dt = maximum allowed voltage slew rate (V/s)
4. The maximum voltage variation between +12 V inputs is ±1.92 V.

A system that supports a PCI Express 150 W / 225 W/300 W add-in card must deliver the +12-V to the standard connector and the additional +12-V via additional auxiliary power supply connector(s), from the same or different rails in the power supply. This is up to the discretion of the system designer. For each 2 x 3 or 2 x 4 auxiliary power connector, the power supplied through the different pins must come from the same rail in the power supply. For add-in card requirements, refer to Chapter 5.

Table 4-2: 150 W / Table 4-2: 225-225 W / 300-300 W Power Supply Rail Requirements

Power Rail	75-75 W Slot	2 x 3 Connector	2 x 4 Connector	Remarks
+12-V				
Voltage Tolerance	±8%	+5/-8%	+5/-8%	Maximum voltage variation between +12-V inputs is

Commented [NM2]: Can this column be deleted?

Formatted Table

Formatted: Highlight

Formatted: Highlight

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: tabletext, Left, Don't suppress line numbers

Formatted: tabletext, Don't suppress line numbers

Formatted: tabletext, Left, Don't suppress line numbers

Formatted: tabletext, Don't suppress line numbers

Supply Current	5.5 A	6.25 A	12.5 A	1.92 V.

~~Implementation~~ IMPLEMENTATION ~~Note~~NOTE

PCI Express Slot Requirements

The ~~75~~ 75 W slot requirements are defined in this specification. PCI Express 150 W / 225 W / 300 W add-in cards must be capable of accommodating the maximum voltage variation between the 75 W slot, 2 x 3 and 2 x 4 connector +12- V inputs.

Formatted: Font: Arial Black, Not Bold

Formatted: Indent: Left: 0", First line: 0", Space Before: 0 pt

Formatted: Font: Arial Black, Not Bold

Formatted: Font: 11 pt

Formatted: Indent: Left: 0", First line: 0", Right: 0", Space After: 3 pt

4.2. Power Consumption

This specification supports multiple card sizes for system implementation. For each size (see Table 9-1~~Table 9-1~~~~Table 9-1~~ for card size definitions), the maximum power consumption is limited at power on until software configures it for high power – see Chapter 6 ~~the Section 6.9~~ of the *PCI Express Base Specification* for information on the power configuration mechanism. The maximum power dissipation for each size is specified as follows:

- A x1 standard height, half-length card is limited to a ~~10~~ 10 W maximum power dissipation.
- A x1 low profile card is limited to a ~~10~~ 10 W maximum power dissipation.
- A x1 standard height, full-length card is limited to a ~~10~~ 10 W maximum power dissipation at initial power up. When the card is configured for high power, by default, it must not exceed ~~a~~ ~~25~~ 25 W maximum power dissipation or optionally it must not exceed ~~a 75~~ 75 W maximum power dissipation. A x4/x8 or a x16 standard height or low profile card is limited to a ~~25~~ 25 W maximum power dissipation at initial power up. When a card is configured for high power, it must not exceed ~~a 75~~ 75 W maximum power dissipation.

Additional Power Considerations:

- Power for cards that support a ~~75~~ 75 W maximum power dissipation can be drawn via a combination of +12-V and +3.3-V rails but each rail draw is limited as defined in Table 4-1~~Table 4-1~~~~Table 4-1~~, and the sum of the draw on the two rails cannot exceed 75 W.
- The card power limits represent the associated system power and cooling capacity for the slot.

The ~~10~~ 10 W limit assumes natural convection cooling in a system that provides air exchanges.

The ~~25~~ 25 W and above limits assume that sufficient cooling is provided to the slot by the cards in the present chassis environment. In general, the power limits above assume a chassis environment with a maximum internal temperature of 55 °C on the primary component side of the card and natural convection cooling in system that provides air exchanges. Implementation of other chassis environments should pay special attention to system level thermal requirements.

PCI Express specifies support for ~~150~~ 150 W- ~~300~~ 300 W cards. For such solutions, implementers should pay special attention to the system level thermal, acoustic, structure, and power delivery requirements.

IMPLEMENTATION NOTE

Power, Thermal, Mechanical and Labeling Considerations

Implementers should pay special attention to the following:

Implementers should ~~read~~ follow ~~Section 6.9~~Chapter 6 ~~Slot Power Limit Control~~ of the *PCI Express Base Specification* ~~to~~ and comprehend how software can control the maximum power that a card can consume ~~provided~~ per slot ~~that a card can consume~~.

After a card is reset, the initial slot power limit value may be lower than the previous one.

High-power implementations may result in increased card weight. Implementations should use appropriately sized connectors and retention mechanisms to insure connector mechanical integrity is not compromised.

To insure optimum performance, it is recommended that card and system implementers refer to the associated PCI Express high-power thermal and mechanical guidelines.

Implementers should read the latest version of the *PCI Express Label Specification* to comprehend how to appropriately label slots and cards to communicate their maximum power capabilities.

Formatted: Space After: 0 pt

Formatted: Font: 11 pt, Bold

Formatted: Font: 11 pt, Bold

Formatted: Font: 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt

Formatted: Space After: 3 pt

Formatted: Space After: 3 pt, Line spacing: single

Commented [NM3]: Where are these guidelines?

4.3. Power Budgeting Capability

The Power Budget Capabilit~~ies register set~~y structure, as defined in the *PCI Express Base Specification~~, Revision 4.0~~*, shall be implemented for (1) cards capable of using more power than initially allowed at power-up (see Section 4.2), and (2) cards utilizing auxiliary power connections (~~150~~ 150 W, ~~225~~ 225 W, ~~300~~ 300 W, etc.).

Sustained Thermal and Maximum Thermal values shall include all thermal power that is produced by the card.

Populated values shall include all power used by the card including power drawn from auxiliary power connections.

For multi-device cards, an instance of the Power Budget Capabilit~~ies register set~~y structure may report power at a device or card level. Thus for multi-device cards, such as a ~~switch~~ Switch with devices behind it, system software must aggregate all instances of the Power Budget Capabilit~~ies register sets~~y structure implemented at or beneath the base device of the card.

TBD: New thermal guidelines to be determined and added when ECN has been submitted.

Update with info from transient power ECR when available.

Commented [NM4]: What's status of thie ECR?Not in 0.5?

Formatted: Highlight

Formatted: Highlight

4.4. Power Supply Sequencing

There is no specific requirement for power supply sequencing of each of the three power supply rails. They may come up or go down in any order. The system, however, must assert the PERST# signal whenever any of the three power rails goes outside of the specifications provided in Table 4-1~~Table 4-1~~~~Table 4-1~~ (refer to Section 02.22.202.1.5 for specific information on the function and proper use of the PERST# signal).

~~Note:~~ If a PCI Express add-in card requires power supply rail sequencing, it is the responsibility of the add-in card designer to provide appropriate circuitry on the add-in card to meet any power supply rail sequencing requirements.

4.5. Power Supply Decoupling

Due to the low level signaling of the PCI Express interface, it is strongly recommended that sufficient decoupling of all power supplies be provided. This is recommended to ensure that power supply noise does not interfere with the recovery of data from a remote upstream PCI Express device. Some basic guidelines to help ensure a quiet power supply are provided below.

~~Note:~~ The following are guidelines only. It is the responsibility of the add-in card designer to properly test the design to ensure that add-in card circuitry does not create excessive noise on power supply or ground signals at the add-in card edge~~-~~fingers.

- The add-in card device decouple value should average 0.01 µF per device V_{cc} pin (for all devices on the add-in card).
- The trace length between a decoupling capacitor and the power supply or ground via should be less then 0.~~2~~2 inches (5.~~08~~08 mm) and be a minimum of 0.~~02~~02 inches (0.~~508~~508 mm) in width.
- A bulk decoupling capacitor (greater than ~~10~~10 µF) is recommended at the add-in card edge finger for each power supply.
- A bulk decoupling capacitor (greater than ~~10~~10 µF) is recommended on each power supply used within a device on the add-in card. This bulk decoupling capacitor should be in close proximity to the add-in card device.

4.6. Electrical Topologies and Link Definitions

The remainder of this chapter describes the electrical characteristics of PCI Express add-in cards. The electrical characteristic at the card interface is defined in terms of electrical budgets. This budget allocation decouples the electrical specification for the system designer and the card vendor and ensures successful communication between the PCI Express signal input and output Links at the system board and add-in card interface. Unless otherwise ~~noted~~indicated, the specifications contained herein apply to all high-speed signals of each interface width definition. The signaling rate for encoded data is 16.0 GT/s, 8.~~0~~0 GT/s, 5.~~0~~0 GT/s, or 2.~~5~~5 GT/s and the signaling is point-to-point. Requirements are called out separately for 16.0 GT/s, 8.~~0~~0 GT/s, 5.~~0~~0 GT/s, and 2.~~5~~5 GT/s signaling rates. CEM motherboards and add-in cards ~~that support the 5.0 GT/s rate must also support the 2.5 GT/s rate. CEM motherboards and add-in cards that support the 8.0 GT/s rate must also support the 5.0 GT/s and 2.5 GT/s rate.~~ must support at least 2.5 GT/s signaling and must support all data rates below the maximum data rate the motherboard or add-in card supports.

4.6.1. Topologies

The electrical topologies supported by this specification are:

- PCI Express devices across one connector on a system with a system board and an add-in card.
- PCI Express devices across two connectors on a system with a system board, a riser card, and an add-in card.

~~Add Implementation note about two connector topologies and retimers. Not strictly data rate dependent but higher rates are more likely to need this.~~

Note: The two connector topologies with higher loss and especially if they support 16 GT/s data rate are likely to need retimers.

- ~~PCI Express devices across two connectors on a system with a system board, a riser card, and an add-in card~~

~~**Note:** The two connector topology is only supported at 16.0 GT/s when a retimer is included on the motherboard. TBD: Need to determine if more details on exact placement of retimer is required.~~

This specification supports only the one and two connector topologies. The "PCI Express on-board" configuration is used for two-PCI Express devices on a common PCB (see Figure 4-1). Since there are no add-in cards involved in this topology, refer to the *PCI Express Base Specification, ~~Revision 4.0~~* for implementation of this topology.

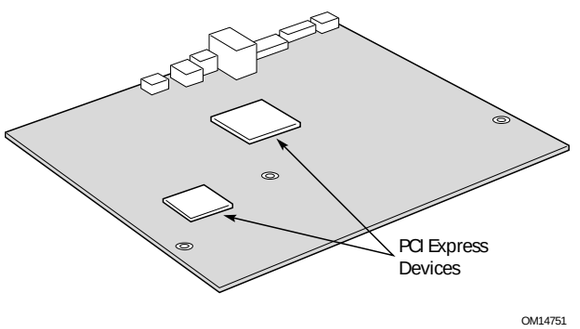


Figure 4-~~14-1~~: PCI Express on the System Board

The topology of "PCI Express with one connector" allows a plug-in PCI Express add-in card similar to a standard PCI or AGP add-in card to interface with a system board using a PCI Express vertical edge connector (Figure 4-2~~Figure 4-2~~~~Figure 4-2~~). In this topology, only one connector-card interface exists~~.~~:

Formatted: Highlight

Formatted: Indent: Left: 0.19", No bullets or numbering

Formatted: Highlight

Formatted: Indent: Left: 0", Hanging: 0.25", No bullets or numbering

Formatted: Bulleted + Level: 1 + Aligned at: 0.44" + Indent at: 0.69"

Formatted: Indent: Left: 0.19", Hanging: 0"

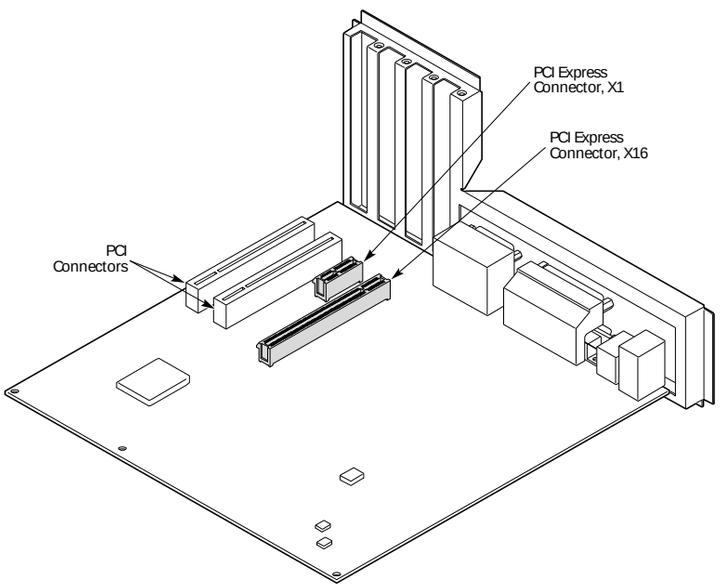


Figure 4-2~~4-2~~: PCI Express Connector on System Board with an Add-in Card

The topology of "PCI Express with two connectors on a riser card" allows for a plug-in PCI Express add-in card similar to a standard PCI or AGP add-in card to interface with a riser card using a PCI Express connector (Figure 4-3~~Figure 4-3~~~~Figure 4-3~~). The riser card plugs to the system board using another riser connector (either PCI Express or other connector). In this topology, two connector-card interfaces exist.

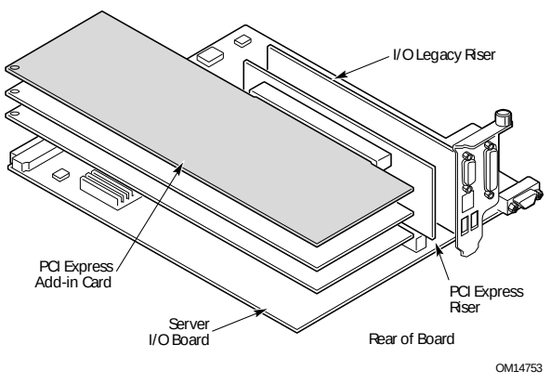


Figure 4-~~34-3~~: PCI Express Connector on a Riser Card with an Add-in Card

4.6.2. Link Definition

Typical PCI Express Links consist of the following:

- Transmitters/Receivers on an ASIC on a system board
- Package fan-in-out trace topologies
- PCB coupled microstrip and/or striplines
- Vias for layer changes
- Optional proprietary PCI Express connector and riser card interface
- Optional riser card with microstrip and/or stripline trace
- PCI Express connector and add-in card interface
- Coupled microstrip line and/or stripline traces on add-in card
- AC-coupling capacitors
- Transmitter/Receivers on an ASIC on the add-in card

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

The electrical parameters for the Link are subdivided into two components (Figure 4-4~~Figure 4-4~~~~Figure 4-4~~):

- Add-in card
- System board and PCI Express connector (and riser card with associated connector if it exists)

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

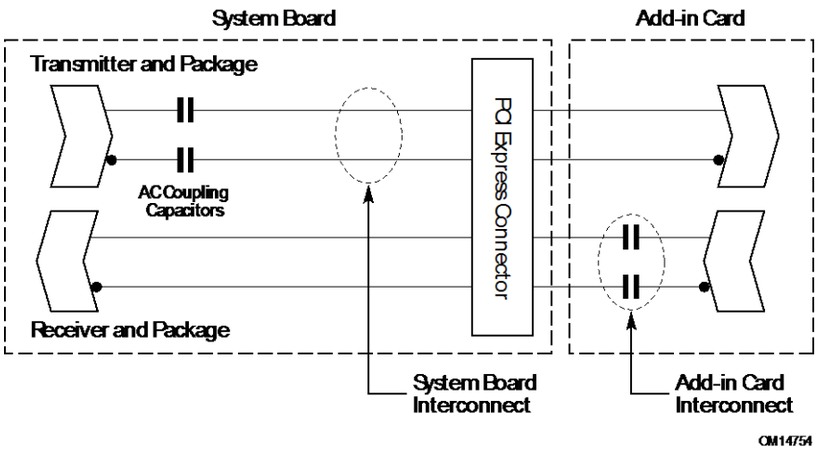


Figure 4-~~4~~4-~~4~~4: Link Definition for Two Components

The electrical impact ~~of discontinuities~~ on the Link due to discontinuities such as vias, bends, and test-points should be included in the respective components.

4.7. Electrical Budgets

A budget is defined for each of the following electrical parameters associated with the Link:

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

- AC coupling capacitors
- Insertion Loss (Voltage Transfer Function)
- Jitter
- Lane-to-Lane skew
- Crosstalk
- Equalization
- Skew within a differential pair
- Differential data trace impedance
- Differential data trace propagation delay
- The electrical budgets are different for each of the two Link components:
- Add-in card budget

- System board and PCI Express connector budgets
- The interconnect Link budget allocations associated with the Transmitters and Receivers differ. This is to account for any electrical characteristics the AC coupling capacitors may contribute to the Link.

4.7.1. AC Coupling Capacitors

The PCI Express add-in card and system board shall incorporate AC coupling capacitors on the Transmitter differential pair. This is to ensure blocking of the DC path between the PCI Express add-in card and the system board. The specific capacitance values are specified in the *PCI Express Base Specification~~, Revision 4.0~~*.

~~Note: ~~Capacitance value requirements are different for 16.0 GT/s and 8.0 GT/s add-in cards and system boards.

~~Note that a~~Attenuation or jitter caused by the coupling capacitors must be accounted for as part of the budget allocation for the physical interconnect component's path on which the capacitors are mounted. ~~Note that t~~There may be parasitic effects associated with the component's placement as mounted on the printed circuit board.

4.7.2. Insertion Loss Values (Voltage Transfer Function)

Appendix A contains background information on maximum insertion loss assumptions that were made in computing the 2.5 GT/s eye diagram requirements. This section is provided only for information purposes.

4.7.3. Jitter Values

The maximum jitter values in terms of percentage of Unit Interval (UI = 400 ps for 2.5 GT/s, 200 ps for 5.0 GT/s, 125 ps for 8.0 GT/s and 62.5 ps for 16.0 GT/s) are specified for the system board and the add-in card. The jitter associated with the riser card and associated proprietary connector will be part of the system board jitter budget. The jitter values are defined with respect to 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the interface (see Figure 4-5~~Figure 4-5~~~~Figure 4-5~~).

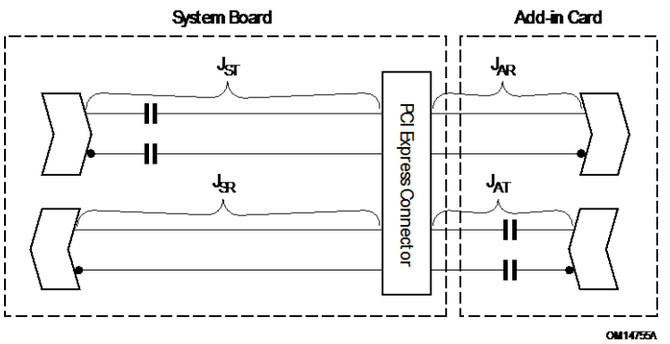


Figure 4-54-5: Jitter Budget

The total system jitter budget is derived with the assumption of a minimum Rj for each of the four budget items. This minimum Rj component is used to determine the overall system budget. The probability distribution of the Rj component is at the Bit Error Rate (BER) indicated and is Gaussian.

For any jitter distribution, the total Tj must always be met at the BER. The Rj of the components are independent and convolve as the root sum square. Tradeoffs of Rj and Dj are allowed, provided the total Tj is always met. More information on the calculation of the system budget can be found in *PCI Express Jitter and BER*.

Table 4-34-2: Total System Jitter Budget for 2.5 GT/s Signaling

Jitter Contribution	Min Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)[3][1]	Tj at BER 10^{-6} (ps)[2]
Tx	2.8	60.6	100	87
Ref Clock	4.7	41.9	108	86
Media	0	90	90	90
Rx	2.8	120.6	160	147
Linear Total Tj:			458	410
Root Sum Square (RSS) Total Tj:			399.13	371.52

Notes:

1. RSS equation for BER 10^{-12} Tj = $\sum Dj_n + 14.069 * \sqrt{\sum Rj_n^2}$

2. RSS equation for BER 10^{-6} Tj = $\sum Dj_n + 9.507 * \sqrt{\sum Rj_n^2}$

[3] This column provides jitter limits at different BER values on a bathtub curve. If bathtub curves are not used in jitter measurements, then the jitter limit in the 10^{-6} column should be used as the total jitter limit for measurements using approximately 10^6 unit intervals of data.

Formatted: Superscript

Formatted: Superscript

2.3. This column provides jitter limits at different BER values on a bathtub curve. If bathtub curves are not used in jitter measurements, then the jitter limit in the 10^{-6} column should be used as the total jitter limit for measurements using approximately 10^6 unit intervals of data.

Table 4-44-3: Allocation of Interconnect Jitter Budget for 2.5 GT/s Signaling

Jitter Parameter	Jitter Budget Value (UI)		Comments
PCI Express Add-in Card	J_{AR} < 0.0575	J_{AT} < 0.0650	Notes 1, 2
System Board and Connector	J_{ST} < 0.1675	J_{SR} < 0.1600	Notes 1, 3
Total Jitter	J_T < 0.225		Note 1

Notes:

1. All values are referenced to 100 Ω, realized as two 50 Ω resistances. The jitter budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.

   The *PCI Express Base Specification, Revision 4.0* allows an interconnect jitter budget of 0.225 UI (equivalent to to 90 ps for a 400 ps Unit-Interval). The allocated jitter budget values in Table 4-3Table 4-3Table 4-2 and Table 4-4Table 4-4Table 4-3 directly correlate to the eye diagram widths in Section 4.8. Tradeoffs in terms of attenuation, crosstalk, and mismatch can be made within the budget allocations specified. No additional guard band is specifically allocated.

   1. The jitter allocations are then assumed per differential pair according to the table. These allocation assumptions must also include any effects of far-end crosstalk.All values are referenced to 100 Ω.

2. The add-in card budget does not include the add-in card edge- finger or connector. However, it does include potential jitter from the AC coupling capacitors on the Transmitter (TX) interconnect of the add-in card. The budget allocations generally allow for a maximum of 4-inch trace lengths for differential pairs having an approximate 0.127 mm (5 mil) trace width. No specific trace geometry, however, is explicitly defined in this specification. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.

3. All values are referenced to 100 Ω. The system board budget includes the PCI Express connector and assumes it is mated with the card edge- finger. Refer to Section 6.3 for specifics on the standalone connector budget. The system board budget includes potential jitter from the AC coupling capacitors on the Transmitter (TX) interconnect on the system board. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.

The total system jitter budget for 5.0 GT/s signaling specifies separate Rj and Dj limits for each of the four components in the jitter budget. Refer to Chapter 9Section 4.3.3.8 in the *PCI Express Base Specification, Revision 4.0* for a more detailed discussion of the system jitter budget, Rj and Dj.

Table 4-54-4: Total System Jitter Budget for 5.0 GT/s Signaling

Jitter Contribution	Max RMS Rj (ps)	Max Dj (ps)	Tj at BER 10^{-12} (ps)[1]
Tx	1.4	30	50
Ref Clock	3.1	0	43.6
Media	0	58	58
Rx	1.4	60	80
Linear Total Tj:			231.6
Root Sum Square (RSS) Total Tj:			200

Formatted: Font: 9 pt, Font color: Black

Commented [NM5]: Notes 2 and 3 present in 2.0 and 1.1 spec. Separated Note-1 to Notes 2 and 3.

Formatted: Font: Hidden

Formatted: Indent: Left: 0.13", No bullets or numbering

Formatted: Font: Hidden

Formatted: Indent: Left: 0.25", No bullets or numbering

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Indent: Left: 0.25", No bullets or numbering

Commented [NM6]: Now will refer to Chapter 7 and not 4 No section refrences- only spec ref and chapter name

Formatted: Superscript

Notes:

1. RSS equation for BER 10^{-12} Tj = $\sum Dj_n$ + 14.069 * $\sqrt{\sum Rj_n^2}$

The total system jitter budget for 8.0 GT/s and 16.0 GT/s signaling does not set separate Rj and Dj limits for all of the four components in the jitter budget. Refer to the *PCI Express Base Specification, ~~Revision 4.0~~* for a more detailed discussion of the system jitter budget at 8.0 GT/s and 16.0 GT/s.

~~Note:~~ The jitter budget distributions above are used to derive the eye diagram widths as described later in this chapter. However, they are provided here only as a design guideline. Compliance measurements must actually be verified against the eye diagrams themselves as defined in Section 4.8~~4.8.4.8~~.

4.7.4. Crosstalk

All add-in card designs must properly account for any crosstalk that may exist among the various pairs of differential signals. Crosstalk may be either near-end (NEXT) or far-end (FEXT). Each component can have potential impact on a design and must be planned for accordingly.

~~Note that t~~The total maximum crosstalk that a Receiver component in Electrical Idle is required to tolerate is with 2.5 GT/s signaling < 65 mV as dictated by the Electrical Idle Detect Threshold in the *PCI Express Base Specification~~, Revision 4.0~~*. Additionally, crosstalk between differential pairs on the add-in card will influence and impact the data signals and any subsequent loss and jitter budgets as ~~noted~~ described in Sections 4.7.2 and 4.7.3. ~~Note that a~~All eye diagrams in Section 4.8 must account for any and all crosstalk present. In order to limit crosstalk impacts and implications, it is recommended that the add-in card limit the total amount of NEXT to a maximum of 50 mV for 2.5 GT/s signaling.

All system boards interfacing with an add-in card must also properly account for crosstalk. The system board must also account for potential crosstalk that can occur on the printed circuit board as well as within the connector itself (see Section 6.3).

4.7.5. Lane-to-Lane Skew

The skew at any point is measured using zero crossings of differential voltage of the compliance pattern, while simultaneously transmitting on all physical Lanes. The compliance pattern is defined in the *PCI Express Base Specification~~, Revision 4.0~~*.

Table 4-~~6~~4-~~5~~: Allowable Interconnect Lane-to-Lane Skew

Skew Parameter	Symbol	Skew Values	Comments
Total Interconnect Skew	S_T	1.6 ns	This does not include Transmitter output skew, $L_{TX\text{-}SKEW}$ (specified in the *PCI Express Base Specification~~, Revision 4.0~~*). The total skew at the Receiver (S_T + $L_{TX\text{-}SKEW}$) is smaller than $L_{RX\text{-}SKEW}$ (specified in the *PCI Express Base Specification~~, Revision 4.0~~*) to minimize latency for this add-in card topology.
PCI Express Add-in Card	S_A	0.35 ns	Estimates about a 2-inch trace length delta on FR4 boards.

Formatted: Font: (Default) Garamond, 12 pt, Not Bold, Font color: Black

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers, Border: Top: (No border), Bottom: (No border), Pattern: Clear

Formatted: Font: (Default) Garamond, 12 pt, Font color: Black

Formatted: Not Highlight

Field Code Changed

System Board	S_s	1.25 ns	Estimates about a 7-inch trace length delta on FR4 boards.

4.7.6. Transmitter Equalization

To reduce ISI, 3.5 dB ~~(±0.5 dB)~~ below the first bit de-emphasis in the Transmitter is required for the add-in card and the system board for 2.5 GT/s signaling. 6.0 dB ~~(±0.5 dB)~~ or 3.5 dB ~~(±0.5 dB)~~ de-emphasis is required for the add-in card and system board for 5.0 GT/s signaling. ~~For implementation details, refer to Chapter 4 in the *PCI Express Base Specification, Revision 4.0.*~~ For add-in cards or system boards that support 8.0 GT/s and / or 16.0 GT/s signaling, refer to the *PCI Express Base Specification, ~~Revision 4.0~~* for equalization preset requirements. For implementation details, refer to Chapter 9 in the *PCI Express Base Specification.* A motherboard must meet eye diagram requirements in Chapter 9 ~~Section 4.8~~ at 8.0 GT/s and ~~Section TBD at~~ 16.0 GT/s on each lane with one or more preset equalization setting.

~~BASE is adding preset test to check for high frequency correctness of Tx presets. Uses eye test at specific presets with different height and width requirements at each preset. Add a table of values to be filled out for .7 spec. Remove note and replace with table of requirements.~~

IMPLEMENTATION NOTE

Preset Test Requirements at 8 GT/s and 16 GT/s

All add-in cards and system boards operating at 8 GT/s and / or 16 GT/s are required to meet the preset test as described in Chapter 9~~Section TBD~~ of the *PCI Express Base sSpecification*. The test consists of acquiring the Tx compliance waveforms from the device under test for each preset then analyzing the waveforms together to confirm that the preset requriements have been met.

Field Code Changed

Formatted: Highlight

Formatted: Highlight

Formatted: Font: Italic

Formatted: Not Highlight

Formatted: Font: Italic

A system board shall meet the following additional rules for this specification:

- The system board initial TX preset at 8.0 GT/s shall be P1, P7, or P8.
- If the equivalent of the ps21 parameter defined in the *PCI Express Base Specification, ~~Revision 4.0~~* measured at data rates of 8.0 GT/s at the end of the 5.0 GT/s System-Board Test Channel without de-embedding shows a loss of more than 12 dB, then the system board initial TX preset at 8.0 GT/s shall be P7 or P8.
- The system board initial Tx preset at 16.0 GT/s shall be P7. Revisit this.
- ~~If the equivalent of the ps21 parameter defined in the *PCI Express Base Specification, Revision 4.0* measured at the end of the 5.0 GT/s System-Board Test Channel without de-embedding shows a loss of more than 12 dB, then the system board initial TX preset at 8.0 GT/s shall be P7 or P8.~~

An add-in card shall meet the following additional rules for this specification:

- If the system board loss is less than 12 dB ~~TX,~~ the add-in card shall receive with a BER of at least E-4 at 8.0 GT/s with presets P1, P7, and P8.
- If the system board loss is more than 12 dB ~~TX~~, the add-in card shall receive with a BER of at least 10^{-4} ~~E-4~~ at 8.0 GT/s with presets P7 and P8.
- The add-in card shall receive with a BER of at least 10^{-4} ~~E-4~~ at 16.0 GT/s with preset P7.

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Commented [NM7]: Defer to 0.7?

Formatted: Highlight

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Superscript

4.7.7. Skew within the Differential Pair

The skew within the differential pair gives rise to a common-mode signal component, which can, in turn, increase Electromagnetic Interference (EMI). The differential pair shall be routed such that the skew within differential pairs is less than 0.~~127~~ 127 mm (~~5~~ 5 mils) for the add-in card and 0.~~254~~ 254 mm (10 mils) for the system board.

4.7.8. Differential Data Trace Impedance

The PCB trace pair differential impedance for a 5.0 GT/s capable data pair must be in the range of 68 Ω to 105 Ω. The PCB trace pair differential impedance for an 8.0 GT/s capable data pair must be in the range of 70 Ω to 100 Ω. The PCB trace pair differential impedance for 16.0 GT/s capable data pair must be in the range of TBD Ω to TBD Ω. These limits apply to both the add-in card and the system board.

Formatted: Highlight

~~Notes~~
~~- Motherboards with long (high loss) channels may need to have tighter impedance control.~~
~~- This requirement does not apply to vias, the connectors, package traces, cables, and other similar structures.~~
~~- Designs should still attempt to minimize the impedance discontinuities from vias, the connectors, package traces, cables, and other similar structures.~~

IMPLEMENTATION NOTE

Differential PCB Trace Impedance

The PCB trace impedance requirement specified in Section 4.7.8 only applies to topologies that support 5.~~0~~ 0 GT/s, 8.0 GT/s or ~~8~~16.~~0~~ 0 GT/s covered by this form factor specification that use the connector defined in this form factor specification.

Specifically, the *PCI Express Card Electromechanical Specification* covers the following two topologies (as defined in Section 4.6.1):

- PCI Express devices across one card electromechanical connector on a system with a system board and an add-in card.
- PCI Express devices across two card electromechanical connectors on a system with a system board, a riser card, and an add-in card, where the connector between the riser card and the add-in card is a card electromechanical connector.

Motherboards with lossy or reflective ~~long (high loss)~~ channels may need to have tighter impedance control. ~~This requirement does not apply to vias, the connectors, package traces, cables, and other similar structures.~~

Designers should ~~still~~ attempt to minimize the impedance discontinuities from vias, the connectors, package traces, cables, and other similar structures.

Further, designers should follow the add-in card and system board layout requirements and recommendations as described in sections 9.2 and 9.3 when developing devices that operate at 16 GT/s.

Other topologies governed by different specifications may impose different impedance requirements or leave the impedance unspecified.

For example, the topology of "PCI Express devices on the same system board" does not fit within a form factor specification and hence must only follow the requirements of the *PCI Express Base Specification*. The *PCI Express Base Specification* does not define a PCB trace impedance requirement so with this topology designers can choose the PCB trace impedance that is best for their applications.

Formatted: Font: 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt, Border: Top: (No border), Bottom: (No border)

Formatted: Font: (Default) Arial, 10 pt

4.7.9. Differential Data Trace Propagation Delay

The propagation delay for an add-in card data trace from the edge ~~-~~finger to the Receiver/Transmitter must not exceed 750 ps.

4.8. Eye Diagrams at the Add-in Card Interface

The eye diagrams defined in this section represent the compliance eye diagrams that must be met for both the add-in card and a system board interfacing with such an add-in card. The specific measurement requirements (probe test points, calibrated system board specifics, etc.) for compliance of physical components are to be specified in the *PHY Electrical Test Considerations for PCI Express Architecture* document. A minimum sample size of 10^6 UI is assumed for the eye diagram measurements at data rates of 2.5 GT/s and 5.0 GT/s. A minimum sample size of 1.~~5X10~~^{6}-$5x10^6$ UI is assumed at data rates of 8.0GT/s and 16.0GT/s. These compliance eye diagrams with BER of 10^{-12} can also be used for simulation by following the guidelines explained in Section 4.7. ~~**Note:**~~ The eye diagrams specified for 5.0 GT/s include de-emphasis jitter affects. De-emphasis jitter is not derated in 5.0 GT/s measurements.

4.8.1. Add-in Card Transmitter Path Compliance Eye Diagram at 2.5 GT/s

The eye diagrams for the add-in card's Transmitter path compliance at 2.5 GT/s are defined in Table 4-7~~Table 4-7~~~~Table 4-6~~ and Figure 4-7~~Figure 4-7~~~~Figure 4-7~~.

Table 4-7~~4-6~~: Add-in Card Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	514	1200	mV	Notes 1, 2, 5
V_{TXA_d}	360	1200	mV	Notes 1, 2, 5
T_{TXA}	287		ps	Notes 1, 3, 5
$J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		56.5	ps	Notes 1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.
4. $J_{TXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in the *PCI Express Base Specification~~, Revision 4.0~~*. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12}.
5. The values in Table 4-7~~Table 4-7~~~~Table 4-6~~ are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card (see Figure 4-5~~Figure 4-5~~~~Figure 4-5~~). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

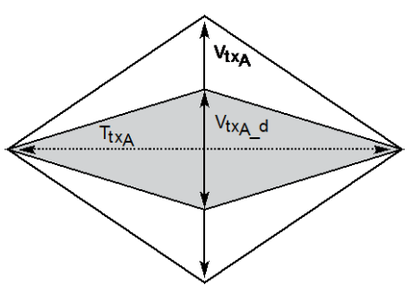


Figure 4-6~~4-6~~: 2.5 GT/s Add-in Card Transmitter Path Compliance Eye Diagram

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

4.8.2. Add-in Card Transmitter Path Compliance Eye Diagrams at 5.0 GT/s

The eye diagrams for the add-in card's Transmitter path compliance at 5.0 GT/s are defined in Table 4-7~~Table 4-7~~~~Table 4-6~~, Table 4-8~~Table 4-8~~~~Table 4-7~~, Table 4-9~~Table 4-9~~~~Table 4-8~~, Table 4-10~~Table 4-10~~~~Table 4-9~~, Table 4-11~~Table 4-11~~~~Table 4-10~~, and Figure 4-7~~Figure 4-7~~~~Figure 4-7~~.

Formatted: Do not check spelling or grammar

Table 4-~~8 4-7~~: Add-in Card Transmitter Path Compliance Eye Requirements at 5.0 GT/s and 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	380	1200	mV	Notes 1, 2, 4
V_{TXA_d}	380	1200	mV	Notes 1, 2, 4
T_{TXA} (with crosstalk)	123		ps	Notes 1, 3, 4
T_{TXA} (without crosstalk)	126		ps	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (*PCI Express Base Specification,* Chapter 4~~*Revision 4.0,* Section 4.2.8~~) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at ~~-~~BER 10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
4. The values in Table 4-8~~Table 4-8~~~~Table 4-7~~ are referenced to an ideal 100 Ω differential load at the end of an isolated 3-inch long 85 Ω differential trace behind a standard PCI Express connector. This channel shall be referenced as the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

The add-in card total jitter for the Transmitter ~~+~~and the Transmitter interconnect must meet the requirements in Table 4-9~~Table 4-9~~~~Table 4-8~~ when decomposed into random and deterministic jitter.

Table 4-~~9 4-8~~: Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 3.5 dB De-emphasis

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	1.4	57	77
Without crosstalk	1.4	54	74

Table 4-10~~4-9~~: Add-in Card Transmitter Path Compliance Eye Requirements at 5.0 GT/s at 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{TXA}	306	1200	mV	Notes 1, 2, 4
V_{TXA_d}	260	1200	mV	Notes 1, 2, 4
T_{TXA} (With crosstalk)	123		ps	Notes 1, 3, 4
T_{TXA} (Without crosstalk)	126		ps	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (*PCI Express Base Specification,* Chapter 4~~*Revision 4.0,* Section 4.2.8~~) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at- BER 10^{-12} must not exceed T_{TXA}. If the add-in card board uses non-interleaved routing, then crosstalk will be present in the measured data. If the add-in card board uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
4. The values in Table 4-10~~Table 4-10~~Table 4-9 are measured using the 5.0 GT/s Add-in Card Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

The add-in card total jitter for the Transmitter and the ~~+~~ Transmitter interconnect must meet the requirements in Table 4-11~~Table 4-11~~Table 4-10 when decomposed into random and deterministic jitter.

Table 4-11~~4-10~~: Add-in Card Jitter Requirements for 5.0 GT/s Signaling at 6.0 dB De-emphasis

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	1.4	57	77
Without crosstalk	1.4	54	74

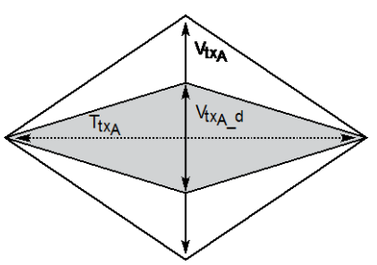


Figure 4-7~~4-7~~: 5.0 GT/s Add-in Card Transmitter Path Compliance Eye Diagram

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Highlight
Formatted: Do not check spelling or grammar
Formatted: Font color: Black
Formatted: Indent: Left: 0", Hanging: 0.75"
Formatted: Font color: Black
Formatted: Font color: Black
Formatted: Font color: Black
Formatted: Font color: Black

4.8.3. Add-in Card Transmitter Path Compliance Eye Diagrams at 8.0 GT/s

The eye diagrams for the add-in card's Transmitter path compliance at 8.0 GT/s are defined in Table 4-12~~Table 4-12~~~~Table 4-11~~. The add-in card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.4.1.2.2~~. The eye diagram requirements are evaluated after the behavioral CDR ~~defined in the *PCI Express Base Specification, Revision 4.0,* Section 4.4.2.1.3~~ and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.4.2.1.4~~ are applied.

Table 4-12~~4-11~~: Add-in Card Transmitter Path Compliance Eye Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	34	1200	mV	Notes 1, 2, 4
V_{TXA_d}	34	1200	mV	Notes 1, 2, 4
T_{TXA}	41.25		ps	Notes 1, 3, 4

Notes:

1. A worst case reference clock with 1 ps RMS jitter is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (*PCI Express Base Specification,* Chapter 4~~*Revision 4.0,* Section 4.2.10~~) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.
4. The values in Table 4-12~~Table 4-12~~~~Table 4-11~~ are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately four inches of 85 ohm trace, followed by a second PCI Express connector, followed by approximately 10.8 inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 8.0 GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. ~~Note that a~~Additional loss from the measurement set-up must be removed. ~~Note that t~~The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

4.8.4. Add-in Card Transmitter Path Pulse Width Jitter at 8.0 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX\text{-}UPW\text{-}TJ}$ and $T_{TX\text{-}UPW\text{-}DJDD}$) at a BER of 10^{-12} are defined in Table 4-13~~Table 4-13~~ . The add-in card shall pass the timing requirements with one of the Tx equalization presets defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.3.3.5.2~~. The optimal preset can be specified by the add-in card developer or an exhaustive test of all presets can be used with the optimal preset defined as that which gives the best values of $T_{TX\text{-}UPW\text{-}TJ}$ and $T_{TX\text{-}UPW\text{-}DJDD}$. The pulse width jitter requirements are evaluated after the behavioral CDR defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.3.4.3.4~~ but with no behavioral RX Equalization applied.

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Subscript, Small caps

Formatted: Subscript, Small caps

Formatted: Superscript

Formatted: Subscript, Small caps

Formatted: Subscript, Small caps

Table 4-13: Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 8.0 GHzGT/s

Parameter	Min	Max	Unit	Comments
$T_{TX-UPW-TJ}$	0	24 (TDBD-needs adj for channel)	ps PP @ BER 10^{-12}	Notes 1, 2, 3
$T_{TX-UPW-DJDD}$	0	12 (TDBD-needs adj for channel)	ps PP @ BER 10^{-12}	Notes 1, 2, 3

Notes:
1. PWJ parameters shall be measured after DDJ separation.
2. Measured with optimized preset value.
3. Measured after short break-out channel. No additional channel embedded.

4.8.4.4.8.5. Add-in Card Transmitter Path Compliance Eye Diagrams at 16.0 GT/s

The eye diagrams for the add-in card's Transmitter path compliance at 16.0 GT/s are defined in Table 4-14Table 4-16Table 4-12. The add-in card shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification,* Chapter 9*Revision 4.0,* Section 4.4.1.2.2. The eye diagram requirements are evaluated after the behavioral CDR defined in the *PCI Express Base Specification, Revision 4.0,* Section 4.4.2.1.3 and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification,* Chapter 9*Revision 4.0,* Section 4.4.2.1.4 are applied.

Table 4-14Table 4-12: Add-in Card Transmitter Path Compliance Eye Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXA}	TBD	1200	mV	Notes 1, 2, 4
V_{TXA_d}	TBD	1200	mV	Notes 1, 2, 4
T_{TXA}	TBD		ps	Notes 1, 3, 4

Notes:
2.1. A worst case reference clock with 1 ps RMS (TBD) jitter is assumed for this revision of the specification. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (*PCI Express Base Specification,* Chapter 4 *Revision 4.0,* Section TBD) is being transmitted during the test.

3.2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXA} and V_{TXA_d}) at a BER of 10^{-6} is TBD mV.

4.3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 21.5X10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.

4. The values in Table 4-12Table 4-12Table 4-11 are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of approximately TBD inches of 85 Ω trace, followed by a reference receiver package all behind a standard PCI Express connector. This channel shall be referenced as the 16.0 GT/s Add-in Card Test Channel. S-parameters for the channel are provided with the specification. Note that aAdditional loss from

Formatted: Font color: Black
Formatted: TableTitle
Formatted: Font color: Black
Formatted: Font color: Black
Formatted Table
Formatted: Highlight
Formatted: Highlight
Formatted: Indent: Left: 0.44"
Formatted: Indent: Left: 0.44", Tab stops: 0.69", Left + Not at 1.25"
Field Code Changed
Commented [NM8]: All TBD's defer to 0.7?
Formatted: Indent: Left: 0.5", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 1" + Tab after: 1.25" + Indent at: 1.25", Tab stops: 0.75", List tab + Not at 1.25"
Formatted: Highlight
Formatted: Highlight
Formatted: Highlight
Formatted: Highlight
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Not Highlight

the measurement set-up must be removed. ~~Note that t~~The Add-in Card Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant motherboard.

5. TBD- Change Table values to include separate limits for each preset- follow direction for Base 4.0

4.8.6. Add-in Card Transmitter Path Pulse Width Jitter at 16.0 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$) at a BER of 10^{-12} are defined in Table 4-15~~Table 4-15~~Table 4-13~~.~~. The add-in card shall pass the timing requirements with one of the Tx equalization presets defined in the *PCI Express Base Specification,* Chpater 9~~*Revision 4.0,* Section TBD~~. The optimal preset can be specified by the add-in card developer or an exhaustive test of all presets can be used with the optimal preset defined as that which gives the best values of $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$. The pulse width jitter requirements are evaluated after the behavioral CDR defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section TBD~~ but with no behavioral RX Equalization applied.

Table 4-15: Add-in Card Transmitter Path Uncorrelated Pulse Width Jitter Requirements at ~~8~~16.0 GT/s~~Hz~~

Parameter	Min	Max	Unit	Comments
$T_{TX-UPW-TJ}$	0	TBD	ps PP @ BER 10^{-12}	Notes 1, 2
$T_{TX-UPW-DJDD}$	0	TBD	ps PP @ BER 10^{-12}	Notes 1, 2

Notes:
1. PWJ parameters shall be measured after DDJ separation.
2. Measured with optimized preset value.

~~4.8.5.~~4.8.7. Add-in Card Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

The minimum sensitivity values for the add-in card's Receiver path compliance at 2.5 GT/s are defined in Table 4-16~~Table 4-16~~Table 4-~~, and a representative eye diagram is shown in Figure 4-9~~Figure 4-9~~Figure 4-9~~.

Table 4-16~~Table 4-13~~: Add-in Card Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

Table 4-17

Parameter	Min	Max	Unit	Comments
V_{RXA}	238	1200	mV	Notes 1, 2, 5
V_{RXA_d}	219	1200	mV	Notes 1, 2, 5
T_{RXA}	246		ps	Notes 1, 3, 5
$J_{RXA-MEDIAN-to-MAX-JITTER}$	77		ps	Notes 1, 4, 5

Notes:

Formatted: Highlight

Formatted: Superscript

Formatted: Font color: Black

Formatted: TableTitle, Don't keep with next

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Indent: Left: 0.44", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 1" + Tab after: 1.25" + Indent at: 1.25", Tab stops: 0.69", List tab + Not at 1.25"

Formatted: Caption,fighead2,fig and tbl,Table Caption,fighead21,fighead22,fighead23,Table Caption1,fighead211,fighead24,Table Caption2,fighead25,fighead212,fighead26,Table Caption3,fighead27,fighead213,Table Caption4,fighead28,fighead214,fighead29,Table Caption5, Keep with next

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{RXA_d}). V_{RXA} and V_{RXA_d} are differential peak-peak output voltages.
3. T_{RXA} is the eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purpose at BER 10^{-12}.
4. $J_{RXA\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in *the PCI Express Base Specification~~, Revision 4.0~~*. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.
5. The values in Table 4-16~~Table 4-16~~~~Table 4-12~~ are initially referenced to an ideal 100 Ω differential load. The resultant values, when provided to the Receiver interconnect path of the add-in card, allow for a demonstration of compliance of the overall add-in card Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median. Exact conditions required for verifying compliance against these values are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

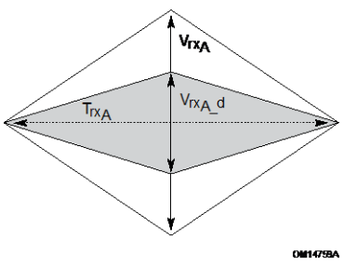


Figure 4-~~8~~4 ~~8~~: 2.5 GT/s Representative Composite Eye Diagram for Add-in Card Receiver Path Compliance

~~4.8.6.~~4.8.8. Add-in Card Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

The minimum sensitivity values for the add-in card's Receiver path compliance at 5.0 GT/s are defined in Table 4-18~~Table 4-18~~~~Table 4-13~~, and a representative eye diagram is shown in Figure 4-9~~Figure 4-9~~~~Figure 4-9~~.

Table 4-~~18~~4 ~~13~~: Add-in Card Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

Parameter	Min	Max	Unit	Comments

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

V_{RXA}	225	1200	mV	Notes 1, 2, 3
V_{RXA_d}	225	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	3.4		ps RMS	
33 kHz Refclk Residual	75		ps PP	
< 1.5 MHz RMS Jitter	4.2		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram. The CMM pattern must be transmitted during the test.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{RXA_d}). V_{RXA} and V_{RXA_d} are differential peak-peak output voltages.
3. The values in Table 4-18~~Table 4-18~~~~Table 4-13~~ are initially calibrated with a reference channel consisting of a 5.0 GT/s Add-in Card Test Channel followed by a 5.0 GT/s System-Board Test Channel. After reference calibration, the 5.0 GT/s System-Board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector. The resultant values, when provided to the Receiver interconnect path of the add-in card, allow for a demonstration of compliance of the overall add-in card Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the add-in card are not specified. The values in Table 4-16~~Table 4-16~~~~Table 4-12~~ may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst case mismatch that could be present with a real system board or the test setup does not provide crosstalk (only a single Lane is tested, etc) the values in Table 4-16~~Table 4-16~~~~Table 4-12~~ must be adjusted accordingly.

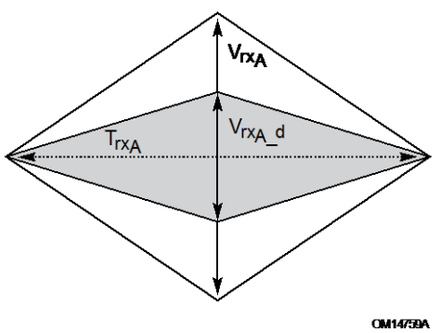


Figure 4-~~9~~4-~~9~~: 5.0 GT/s Representative Composite Eye Diagram for Add-in Card Receiver Path Compliance

~~4.8.7.~~4.8.9. Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the add-in card's Receiver path compliance at 8.~~0~~ 0 GT/s are defined in Table 4-19~~Table 4-19~~~~Table 4-14~~. The receiver path shall be tested with a worst case eye in order to verify that it achieves a BER < 10^{-12}. This worst case eye is calibrated using TX

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Check spelling and grammar
Formatted: Check spelling and grammar
Formatted: Check spelling and grammar

equalization settings that are optimal with the reference equalizer for each calibration channel. After calibration, the test-generator's TX equalization may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst case cross-talk that would be present with all lanes active – the additional cross-talk must be accounted for in some other way.

~~**Note:** If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.~~

~~If the test is not run in a way that produces the worst case cross-talk that would be present with all lanes active – the additional cross-talk must be accounted for in some other way.~~

Formatted: Border: Top: (No border), Bottom: (No border), Pattern: Clear

The test is performed with two different test channels, a long test channel and a short test channel.

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its transmitter equalization is tested by applying a signal whose equalization level is suboptimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. ~~Note that i~~If the RX under test is more capable than the reference (CTLE+DFE) receiver, the RX under test may not require the TX to change its equalization levels to achieve a BER < 10^{-12}. In any case, equalization settings resulting from this procedure shall be used for the above RX test and if the RX requires the TX equalization to change, such change shall be accommodated by the test set-up used.

Formatted: Not Highlight

A specific methodology for this procedure is outside the scope of this specification. Refer to compliance program test procedures for specific test equipment for specific methodology details.

Table 4-~~19~~4-~~14~~: Long Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Formatted: Font color: Black

Formatted: Font color: Black

Parameter	Min	Max	Unit	Comments
$V_{RX\text{-}EH\text{-}8G}$ Eye Height	34	34	mV	Notes 1, 2, 4
$T_{RX\text{-}EH\text{-}8G}$ Eye Width	0.33	0.38	UI	Notes 1, 2
Rj (Random Jitter)	3		ps RMS	Notes 5, 6
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are in reference to BER = 10^{-12}.
2. The values in ~~Table 4-19~~~~Table 4-19~~~~Table 4-14~~ are initially calibrated with a reference channel consisting of an 8.0 GT/s Add-in Card Test Channel followed by an 8.0 GT/s System-Board Test Channel at the TX SMP

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 8.0 GT/s TX test. After reference calibration, the 8.0 GT/s System-Board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector.

3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.

Table 4-~~204~~ ~~15~~: Short Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX-EH-8G}$ Eye Height	N/A	N/A	mV	Notes 1, 2, 5
$T_{RX-EH-8G}$ Eye Width	N/A	N/A	UI	Notes 1, 2, 5
Rj (Random Jitter)	3		ps RMS	Note 4
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are in reference to a BER = 10^{-12}.
2. The values in Table 4-~~20~~15 are initially calibrated with a reference channel consisting of a 5.0 GT/s Add-in Card Test Channel followed by a 5.0 GT/s System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 5.0 GT/s TX test. After reference calibration, the 5.0 GT/s System-board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector.
3. Eye height and width are specified after application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
5. For the short channel test, the calibrated test equipment transmitter settings from the long channel test are used. Eye height and eye width are not separately re-calibrated.

~~4.8.8.~~4.8.10. Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the add-in card's Receiver path compliance at 16.0 GT/s are defined in Table 4-19~~Table 4-21~~~~Table 4-21~~~~Table 4-19~~~~Table 4-14~~. The receiver path shall be tested with a worst case eye in order to verify that it achieves a BER < 10^{-12}. This worst case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for each calibration channel. After calibration, the test-generator's TX equalization may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

If the test is not run in a way that produces the worst case cross-talk that would be present with all lanes active – the additional cross-talk must be accounted for in some other way.

~~**Note:** If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.~~

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

Formatted: Border: Top: (No border), Bottom: (No border), Pattern: Clear

~~If the test is not run in a way that produces the worst case cross-talk that would be present with all lanes active – the additional cross-talk must be accounted for in some other way.~~

The test is performed with two different test channels, a long test channel and a short test channel. ~~TBD: Does Gen 4 still specify two Rx reference channels? Update based on Base Spec.~~

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its transmitter equalization is tested by applying a signal whose equalization level is suboptimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. ~~Note that i~~If the RX under test is more capable than the reference (CTLE+DFE) receiver, the RX under test may not require the TX to change its equalization levels to achieve a BER < 10^{-12}. In any case, equalization settings resulting from this procedure shall be used for the above RX test and if the RX requires the TX equalization to change, such change shall be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification. Refer to compliance program test procedures for specific test equipment and specific methodology details.

Table 4-~~21~~4-~~14~~: Long Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX\text{-}EH\text{-}16G}$ Eye Height	~~TBD~~15	~~TBD~~15	mV	Notes 1, 2, 4
$T_{RX\text{-}EH\text{-}16G}$ Eye Width	~~TBD~~0.3	~~TBD~~0.3	UI	Notes 1, 2
Rj (Random Jitter)	TBD		ps RMS	Notes 5, 6
Sj (Sinusoidal Jitter) 100 MHz	TBD		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	TBD		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are in reference to BER = 10^{-12}.
2. The values in ~~Table 4-19~~Table 4-~~21~~19Table 4-14 are initially calibrated with a reference channel consisting of an ~~8~~16.0 GT/s Add-in Card Test Channel followed by an 16~~8~~.0 GT/s System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 16~~8~~.0 GT/s TX test. After reference calibration, the 16~~8~~.0 GT/s System-Board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at ~~3~~TBD~~1.0~~ ps RMS, it may be adjusted to meet the value for $T_{RX\text{-}EH\text{-}8G\text{-}16G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.

Formatted: Not Highlight

Formatted: Not Highlight

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt, Check spelling and grammar

Formatted: Highlight

Formatted: Highlight

Table 4-224-15: Short Channel Add-in Card Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX\text{-}EH\text{-}16\text{-}SC8G}$ Eye Height	N/A	N/A	mV	Notes 1, 2, 5
$T_{RX\text{-}EH\text{-}16\text{-}SC8G}$ Eye Width	N/A	N/A	UI	Notes 1, 2, 5
Rj (Random Jitter)	TBD		ps RMS	Note 4
Sj (Sinusoidal Jitter) 100 MHz	TBD		ps PP	
Differential Mode Sinusoidal Interference 2.1 GHz	TBD		mV PP	Note 3

Notes:

1. An ideal reference clock without jitter is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are in reference to a BER = 10^{-12}.
2. The values in Table 4-2215 are initially calibrated with a reference channel consisting of a 516.0 GT/s Add-in Card Test Channel followed by a 516.0 GT/s System-Board Test Channel at the TX SMP connectors on the System-Board Test Channel. The calibration is done with the same post processing as the System Board 5.0 GT/s TX test. After reference calibration, the 5.0 GT/s System-board Test Channel is removed and the add-in card to be tested is placed into a standard PCI Express connector.
3. Eye height and width are specified after application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Rj is applied over the following range. The low frequency limit may be between 1.5 MHz and 10 MHz, and the upper limit is 1.0 GHz.
5. For the short channel test, the calibrated test equipment transmitter settings from the long channel test are used. Eye height and eye width are not separately re-calibrated.

4.8.9.4.8.11. System Board Transmitter Path Compliance Eye Diagram at 2.5 GT/s

TBD: This section will need to be replaced if all system compliance testing is converted to using Dual Port or CDR with SSC tracking.

The eye diagram for the system board's Transmitter compliance at 2.5 GT/s is defined in Table 4-22Table 4-23Table 4-16 and Figure 4-12Figure 4-10Figure 4-10Figure 4-12Figure 4-12.

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't suppress line numbers

Formatted: TableTitle, Left, Space Before: 0 pt, After: 0 pt, Don't suppress line numbers

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't suppress line numbers

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Left, Space Before: 0 pt, After: 0 pt, Don't suppress line numbers

Formatted: TableTitle, Right: 0", Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Left, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Right: 0", Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Left, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Right: 0", Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Left, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Right: 0", Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Left, Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Right: 0", Space Before: 0 pt, After: 0 pt, Don't keep with next, Don't suppress line numbers

Formatted: TableTitle, Indent: Left: 0", Space Before: 0 pt, After: 0 pt, Don't suppress line numbers

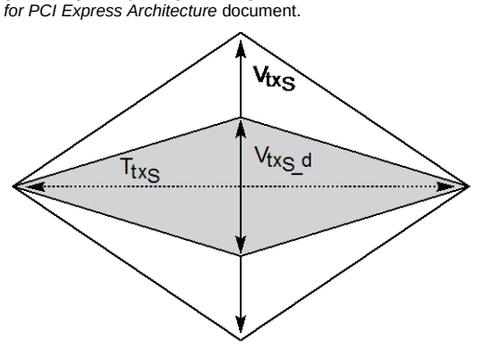
Formatted: TableTitle, Right: 0", No bullets or numbering, Don't suppress line numbers

Formatted: TableTitle, Right: 0", No bullets or numbering, Don't suppress line numbers, Tab stops: Not at 0.31"

Table 4-22234-16: System Board Transmitter Path Compliance Eye Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXS}	274	1200	mV	Notes 1, 2, 5
V_{TXS_d}	253	1200	mV	Notes 1, 2, 5
T_{TXS}	246		ps	Notes 1, 3, 5
$J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$		77	ps	Notes 1, 4, 5

Notes:
1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 233 ps for simulation purposes at BER 10^{-12}.
4. $J_{TXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-max jitter outlier as defined in *the PCI Express Base Specification, Revision 4.0*. The sample size for this measurement is 10^6 UI. This value can be increased to 83.5 ps for simulation purpose at BER 10^{-12}.
5. The values in Table 4-22Table 4-23Table 4-16 are referenced to an ideal 100 Ω differential load at the end of the interconnect path at the edge-finger boundary on the add-in card when mated with a connector (see Figure 4-5Figure 4-5Figure 4-5). The eye diagram is defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.



A-0335

Figure 4-104-10: 2.5 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt

~~4.8.10.~~4.8.12. System Board Transmitter Path Compliance Eye Diagram at 5.0 GT/s

The system board Transmitter path measurements at 5.0 GT/s are made using a two port measurement methodology. Figure 4-11~~Figure 4-11~~~~Figure 4-11~~ shows a functional block diagram for a system board and add-in card that shows the measurement points for the two port method.

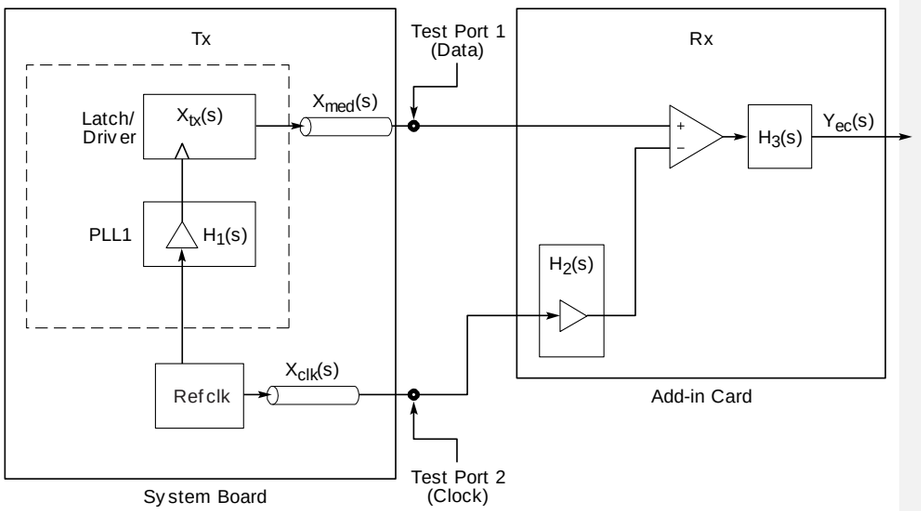


Figure 4-~~11~~14~~-11~~: 5.0 GT/s Two Port Measurement Functional Block Diagram

Equations for the jitter at test port 1 and test port 2 and the eye closure at the add-in card Receiver from the test port signals are provided as follows:

Data Port Measurement (Test Port 1):

Eq.(1) $$X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

Clock Port Measurement (Test Port 2):

Eq.(2) $$X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

Eye Closure At Receiver Due to Signals At Clock and Data Ports:

$$\text{Eq.(3)}\quad Y_{ec}(s)=\{[X_{clk}(s)H_1(s)e^{-sT_{d1a}}+X_{tx}(s)+X_{med}(s)]-[X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}]\}\bullet H_3(s)$$
$$=(X_{dm}(s)-X_{clk}(s)H_2(s)e^{-sT_{d2}})\bullet H_3(s)$$

Where $X_{clk}(s)$ is the reference clock transfer function, T_{d1a} is the delay from the reference clock to the data port, T_{d1b}, is the delay from the reference clock to the test port, $X_{tx}(s)$ is the driver/latch transfer function, and $X_{med}(s)$ is the interconnect transfer function. Where the RX PLL transfer function $H_2(s)$ and the PI transfer function $H_3(s)$ are the same as those defined in the *PCI Express Base Specification~~, Revision 4.0~~* with parameters that give rise to the largest eye closure $Y_{ec}(s)$. The delay T_{d2} is swept from –3 ns to 3 ns – consistent with the maximum transport delay that can occur in the add-in card.

The two port measurement methodology is performed according to the following steps:

- Data is gathered from test port 1 and test port 2 to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
- The eye closure $Y_{ec}(s)$ or Y_{ec} (t) is calculated based on equation 3. T_{d2} is swept from -3 ns to 3 ns. $H_3(s)$ is defined in Chapter 9 ~~Figure 4-21~~ of the *PCI Express Base Specification~~, Revision 4.0~~*. $H_2(s)$ is one of the following values:

$$H_2(s)=\frac{2\zeta\omega_{n2}s+\omega_{n2}^2}{s^2+2\zeta\omega_{n2}s+\omega_{n2}^2}$$

$$where:\zeta=0.54\,(3\,dB\,PK),\ \omega_{n2}=8.61*2\pi\,(16MHz\,3dB\,BW)\ \ Mrad/s \text{ or}$$
$$\zeta=0.54\,(3\,dB\,PK),\ \omega_{n2}=4.31*2\pi\,(8\ Mhz\ 3dB\,BW)\,Mrad/s \text{ or}$$
$$\zeta=1.16\,(1\,dB\,PK),\ \omega_{n2}=1.82*2\pi\,(5\ MHz\ 3dB\,BW)\,Mrad/s$$

- Calculate the eye closure at BER=10^{-12} based on Y_{ec} (t). The maximum eye closure for any parameters of $T_{d2\ and}$ $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter~~,~~ + Transmitter interconnect, and the ~~+~~ reference clock.

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Table 4-~~23~~24~~4~~ ~~17~~: System Board Transmitter Path Compliance Eye Requirements at 5.0 GT/s

Parameter	Min	Max	Unit	Comments
V_{TXS}	225	1200	mV	Notes 1, 2, 4
V_{TXS_d}	225	1200		Notes 1, 2, 4
T_{TXS} (with crosstalk)	95		ps	Notes 1, 3, 4
T_{TXS} (without crosstalk)	108		ps	

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that CMM pattern (*PCI Express Base Specification*, Chapter 4, ~~*Revision 43.0*~~) is being transmitted during the test using the de-emphasis level that the system board will use in normal operation.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXS_d}). V_{TXS} and V_{TXS_d} are minimum differential peak-peak output voltages.
3. T_{TXS} is the minimum eye width. The recommended sample size for the dual port measurement is at least 10^6 UI. The minimum eye opening at BER 10^{-12} is calculated based on the measured data and must not exceed T_{TXS}. If the system board uses non-interleaved routing, then crosstalk will be present in the measured data. If the system uses interleaved routing, then crosstalk will not be present and an adjusted minimum eye width is used.
4. The values in Table 4-23~~Table 4-24~~~~Table 4-17~~ are referenced to an ideal 100 Ω differential load at the end of an isolated 2-inch 85 Ω differential trace behind a standard PCI express edge finger. This channel shall be referenced as the 5.0 GT/s System Board Test Channel. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

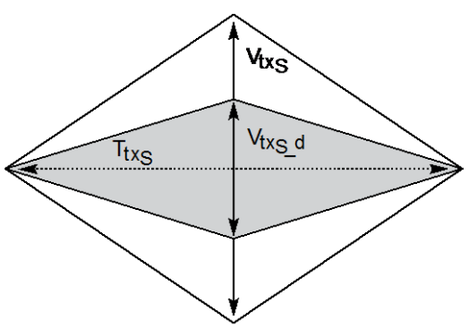


Figure 4-~~12~~4~~ 12~~: 5.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

Formatted: Font: Not Italic

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

The system board total jitter for the transmitter, ~~+~~ transmitter interconnect and the~~+~~ reference clock must meet the requirements in Table 4-24~~Table 4-25~~~~Table 4-18~~ when decomposed into random and deterministic jitter.

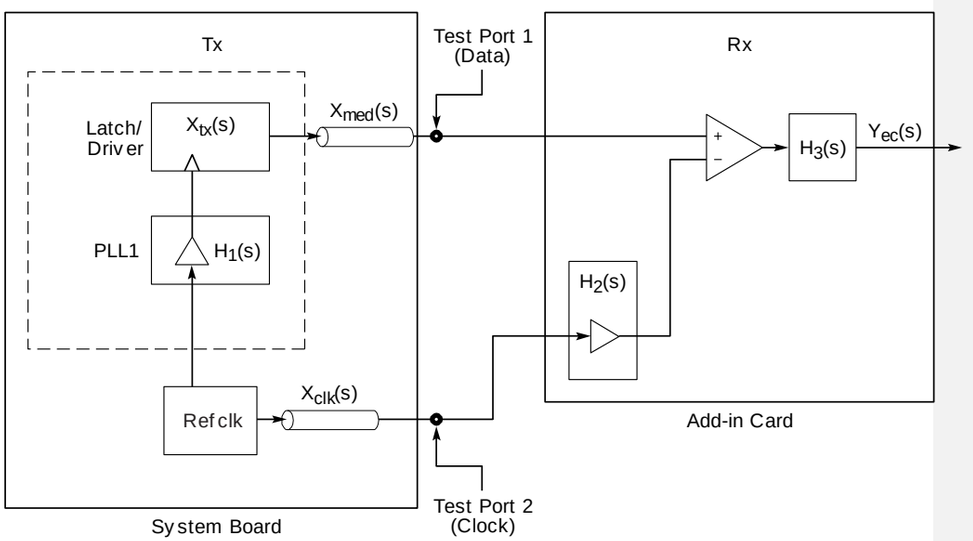
Table 4-~~242~~54-~~18~~: System Board Jitter Requirements for 5.0 GT/s Signaling

	Max Rj (ps RMS)	Max Dj (ps)	Tj at BER 10^{-12} (ps)
With crosstalk	3.41	57	105
Without crosstalk	3.41	44	92

~~4.8.11.~~4.8.13. System Board Transmitter Path Compliance Eye Diagram at 8.0 GT/s

- The system board shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.4.1.2.2~~. The eye diagram requirements are evaluated after the behavioral CDR ~~defined in the *PCI Express Base Specification,* Chapter 9*Revision 4.0,* Section 4.4.2.1.3~~ and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification,* Chapter 9 ~~*Revision 4.0,* Section 4.4.2.1.4~~ are applied.

The system board Transmitter path measurements at 8.0 GT/s are made using a two port measurement methodology. Figure 4-13~~Figure 4-13~~~~Figure 4-13~~ shows a functional block diagram for a system board and add-in card that shows the measurement points for the two port method.



A-0618

Figure 4-~~134~~ ~~13~~: 8 GT/s Two Port Measurement Functional Block Diagram

Equations for the jitter at test port 1 and test port 2 and the eye closure at the add-in card Receiver from the test port signals are provided as follows:

Data Port Measurement (Test Port 1):

$$\text{Eq.(1)} \qquad X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

Clock Port Measurement (Test Port 2):

$$\text{Eq.(2)} \qquad X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

Eye Closure At Receiver Due to Signals At Clock and Data Ports:

$$\text{Eq.(3)} \quad Y_{ec}(s) = \{[X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}]\} \bullet H_3(s)$$

$$= (X_{dm}(s) - X_{clk}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s)$$

Where $X_{clk}(s)$ is the reference clock transfer function, T_{d1a} is the delay from the reference clock to the data port, T_{d1b} is the delay from the reference clock to the test port, $X_{tx}(s)$ is the driver/latch transfer function, and $X_{med}(s)$ is the interconnect transfer function. Where the RX PLL transfer function $H_2(s)$, and PI transfer function $H_3(s)$ are the same as those defined in the *PCI Express Base Specification~~, Revision 4.0~~* with parameters that give rise to the largest eye closure $Y_{ec}(s)$. The delay T_{d2} is swept from –3 ns to 3 ns – consistent with the maximum transport delay that can occur in the add-in card.

The two port measurement methodology is performed according to the following steps:

- Data is gathered from test port 1 and test port 2 to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
- The eye closure $Y_{ec}(s)$ or $Y_{ec}(t)$ is calculated based on equation 3. T_{d2} is swept from -3 ns to 3 ns. $H_3(s)$ is defined in ~~Figure 4-21~~Chapter 9 of the *PCI Express Base Specification~~, Revision 4.0~~*. $H_2(s)$ is one of the following values:

$$H_2(s) = \frac{2\zeta\omega_{n2}s + \omega_{n2}^2}{s^2 + 2\zeta\omega_{n2}s + \omega_{n2}^2}$$

$$where: \zeta = 0.73\,(2\ dB\ PK),\ \omega_{n2} = 6.1\,(2\ MHz\ 3dB\ BW)\ \ Mrad/s \text{ or}$$

$$\zeta = 0.73\,(2\ dB\ PK),\ \omega_{n2} = 12.2\,(4\ Mhz\ 3dB\ BW)\ Mrad/s \text{ or}$$

$$\zeta = 1.15\,(1\ dB\ PK),\ \omega_{n2} = 11.53\,(5\ Mhz\ 3dB\ BW)\ Mrad/s$$

- Calculate the eye closure at BER = 10^{-12} based on $Y_{ec}(t)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter~~,~~ + Transmitter interconnect and the~~+~~ reference clock.

Table 4-~~25264-19~~: System Board Transmitter Path Compliance Eye Requirements at 8.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	34	1200	mV	Notes 1, 2, 4
V_{TXS_d}	34	1200		Notes 1, 2, 4
T_{TXS}	41.25		ps	Notes 1, 3, 4

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (*PCI Express Base Specification*, Chapter 4 ~~*Revision 4.0*, Section 4.2.10~~) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.

~~6.~~4. The values in Table 4-25~~Table 4-26Table 4-19~~ are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of 4.0 inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The s-parameters for the channel are provided with this specification. ~~Note that a~~Additional loss from the measurement set-up must be removed. ~~Note that t~~The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

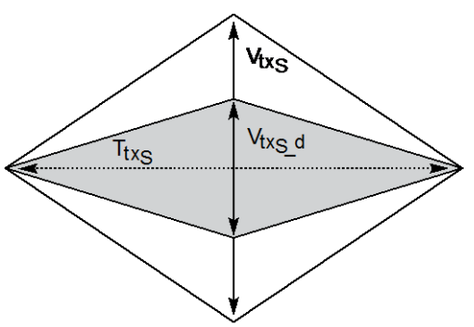


Figure 4-~~144-14~~: 8.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

4.8.14. System Board Transmitter Path Pulse Width Jitter at 8.0 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX\text{-}UPW\text{-}TJ}$ and $T_{TX\text{-}UPW\text{-}DJDD}$) at a BER of 10^{-12} are defined in Table 4-13~~Table 4-13~~ . The add-in card shall pass the timing requirements

Formatted: Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 0.25" + Indent at: 0.5"

Formatted: Right: 0.31", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 0.25" + Indent at: 0.5"

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Highlight

Commented [NM9]: Is PWJ valid after applying ref EQ? Open for 0.5 (Add a note for 0.5)

Formatted: Highlight

with one of the Tx equalization presets defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.3.3.5.2~~. The optimal preset can be specified by the add-in card developer or an exhaustive test of all presets can be used with the optimal preset defined as that which gives the best values of $T_{TX\text{-}UPW\text{-}TJ}$ and $T_{TX\text{-}UPW\text{-}DJDD}$. The pulse width jitter requirements are evaluated after the behavioral CDR defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.3.4.3.4~~. Because of the length of the channel from the system board Tx to the measurement point (Tx SMP connectors on the CLB) behavioral RX Equalization, specifically CTLE, may need to be applied in order to get reliable results. Similarly, the maximum pulse width jitter limits may be increased in order to accommodate the longer channel.

Table 4-~~26~~27: System Board Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 8.0 GHz

Parameter	Min	Max	Unit	Comments
$T_{TX\text{-}UPW\text{-}TJ}$	0	~~30~~TBD	ps PP @ BER 10^{-12}	Notes 1, 2, 3
$T_{TX\text{-}UPW\text{-}DJDD}$	0	~~15~~TBD	ps PP @ BER 10^{-12}	Notes 1, 2, 3

Notes:
1. PWJ parameters shall be measured after DDJ separation.
2. Measured with optimized preset value.
3. Appropriate CTLE Rx equalization will be applied to allow reliable measurement of pulse width jitter.

~~4.8.12.~~4.8.15. System Board Transmitter Path Compliance Eye Diagram at 16.0 GT/s

- The system board shall pass the eye diagram requirements with at least one of the TX equalization presets defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section TBD~~. The eye diagram requirements are evaluated after the behavioral CDR ~~defined in the *PCI Express Base Specification,* Chapter 9*Revision 4.0,* Section TBD~~ and the behavioral RX Equalization Algorithm defined in the *PCI Express Base Specification,* ~~*Revision 4.0,* Section TBD~~Chpater 9 are applied.

The system board Transmitter path measurements at 16.0 GT/s are made using a two port measurement methodology. Figure 4-13~~Figure 4-13~~~~Figure 4-13~~ shows a functional block diagram for a system board and add-in card that shows the measurement points for the two port method.

Formatted: Font: Not Italic

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: TableTitle, Don't keep with next

Formatted Table

Formatted: Highlight

Formatted: Highlight

Formatted: Indent: Left: 0.44", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 1" + Tab after: 1.25" + Indent at: 1.25", Tab stops: 0.69", List tab + Not at 1.25"

Formatted: Not Highlight

Formatted: Not Highlight

Formatted: Font: Not Italic

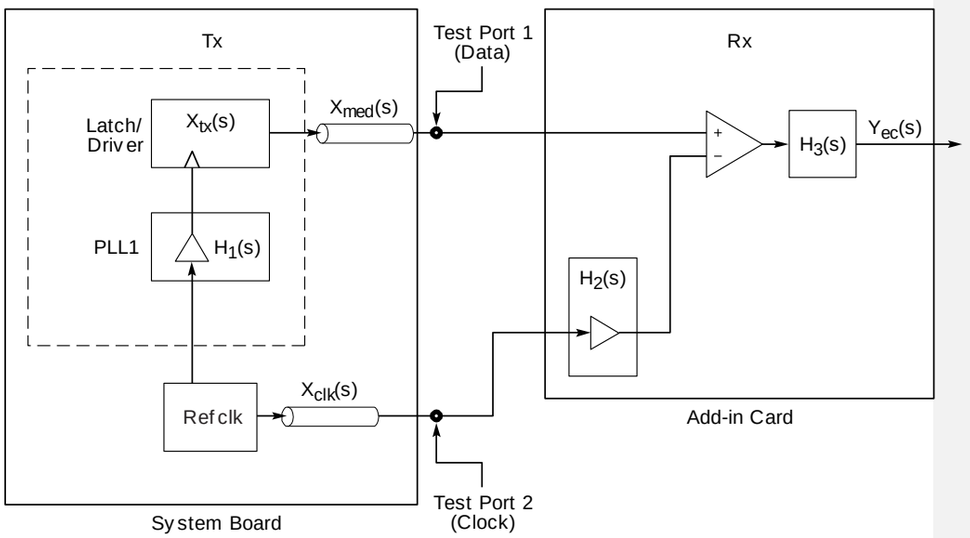


Figure 4-154-15: 16 GT/s Two Port Measurement Functional Block Diagram

Equations for the jitter at test port 1 and test port 2 and the eye closure at the add-in card Receiver from the test port signals are provided as follows:

Data Port Measurement (Test Port 1):

$$\text{Eq.(1)} \qquad X_{dm}(s) = X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)$$

Clock Port Measurement (Test Port 2):

$$\text{Eq.(2)} \qquad X_{cm}(s) = X_{clk}(s)e^{-sT_{d1b}}$$

Eye Closure At Receiver Due to Signals At Clock and Data Ports:

$$\text{Eq.(3)} \quad Y_{ec}(s) = \{[X_{clk}(s)H_1(s)e^{-sT_{d1a}} + X_{tx}(s) + X_{med}(s)] - [X_{clk}(s)e^{-sT_{d1b}}][H_2(s)e^{-sT_{d2}}]\} \bullet H_3(s)$$

$$= (X_{dm}(s) - X_{clk}(s)H_2(s)e^{-sT_{d2}}) \bullet H_3(s)$$

Where $X_{clk}(s)$ is the reference clock transfer function, T_{d1a} is the delay from the reference clock to the data port, T_{d1b} is the delay from the reference clock to the test port, $X_{tx}(s)$ is the driver/latch transfer function, and $X_{med}(s)$ is the interconnect transfer function. Where the RX PLL transfer function $H_2(s)$, and PI transfer function $H_3(s)$ are the same as those defined in the *PCI Express Base Specification*~~, Revision 4.0~~ with parameters that give rise to the largest eye closure $Y_{ec}(s)$. The delay T_{d2} is swept from –3 ns to 3 ns – consistent with the maximum transport delay that can occur in the add-in card.

The two port measurement methodology is performed according to the following steps:

- Data is gathered from test port 1 and test port 2 to obtain the spectrum $X_{dm}(s)$ and $X_{cm}(s)$ or equivalent.
- The eye closure $Y_{ec}(s)$ or $Y_{ec}(t)$ is calculated based on equation 3. T_{d2} is swept from -3 ns to 3 ns. $H_3(s)$ is defined in Figure 4-21 of the *PCI Express Base Specification*~~, Revision 4.0~~. $H_2(s)$ is one of the following values:

$$H_2(s) = \frac{2\zeta\omega_{n2}s + \omega_{n2}^2}{s^2 + 2\zeta\omega_{n2}s + \omega_{n2}^2}$$

$$where: \zeta = 0.73\,(2\ dB\ PK),\ \omega_{n2} = 6.1\,(2\ MHz\ 3dB\ BW)\ \ Mrad/s \text{ or}$$

$$\zeta = 0.73\,(2\ dB\ PK),\ \omega_{n2} = 12.2\,(4\ Mhz\ 3dB\ BW)\ Mrad/s \text{ or}$$

$$\zeta = 1.15\,(1\ dB\ PK),\ \omega_{n2} = 11.53\,(5\ Mhz\ 3dB\ BW)\ Mrad/s$$

- Calculate the eye closure at BER = 10^{-12} based on $Y_{ec}(t)$. The maximum eye closure for any parameters of T_{d2} and $H_2(s)$ in the defined ranges is the total jitter assigned to the system board Transmitter~~,~~ ~~+~~ Transmitter interconnect and the~~+~~ reference clock.

Table 4-27284-19: System Board Transmitter Path Compliance Eye Requirements at 16.0 GT/s with Ideal Adaptive TX Equalization

Parameter	Min	Max	Unit	Comments
V_{TXS}	TBD20.0	1200	mV	Notes 1, 2, 4
V_{TXS_d}	TBD20.0	1200		Notes 1, 2, 4
T_{TXS}	TBD22.0		ps	Notes 1, 3, 4

Notes:

1. All Links are assumed active while generating this eye diagram. The eye diagram requires that the compliance pattern in 128b/130b (*PCI Express Base Specification, ~~Revision 4.0,~~* ~~Section 4.2.10~~Chapter 4) is being transmitted during the test.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{TXA_d}). V_{TXA} and V_{TXA_d} are minimum differential peak-peak output voltages. The voltage measurements are done at a BER of 10^{-12}. For lab use, an informative voltage limit (V_{TXS} and V_{TXS_d}) at a BER of 10^{-6} is 46 mV.
3. T_{TXA} is the minimum eye width. The recommended sample size for this measurement is at least 10^6 UI. This calculated eye width at BER 10^{-12} must not exceed T_{TXA}.
4. The values in ~~Table 4-25~~~~Table 4-26~~~~Table 4-19~~ are referenced to an ideal 100 Ω differential load at the end of an isolated (no crosstalk) test channel consisting of ~~4.0~~TBD inches of 85 Ω trace, followed by a reference receiver package behind a standard PCI Express edge finger. This channel shall be referenced as the 8.0 GT/s System-Board Test Channel. The s-parameters for the channel are provided with this specification. ~~Note that a~~Additional loss from the measurement set-up must be removed. ~~Note that th~~The System-Board Test Channel is a reference channel for testing and does not represent the worst possible channel that could be implemented on a CEM compliant add-in card.

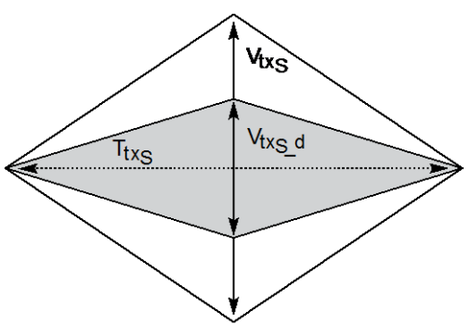


Figure 4-164-16: 16.0 GT/s System Board Transmitter Path Composite Compliance Eye Diagram

Formatted: Font: Not Italic

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

Formatted: Highlight

Formatted: Not Highlight

Formatted: Not Highlight

4.8.16. System Board Transmitter Path Pulse Width Jitter at 16.0 GT/s

The Uncorrelated Total and Deterministic Pulse Width Jitter ($T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$) at a BER of 10^{-12} are defined in Table 4-28~~Table 4-29~~Table 4-13~~.~~. The add-in card shall pass the timing requirements with one of the Tx equalization presets defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.3.3.5.2~~. The optimal preset can be specified by the add-in card developer or an exhaustive test of all presets can be used with the optimal preset defined as that which gives the best values of $T_{TX-UPW-TJ}$ and $T_{TX-UPW-DJDD}$. The pulse width jitter requirements are evaluated after the behavioral CDR defined in the *PCI Express Base Specification,* Chapter 9~~*Revision 4.0,* Section 4.3.4.3.4~~. Because of the length of the channel from the system board Tx to the measurement point (Tx SMP connectors on the CLB) behavioral RX Equalization, specifically CTLE, may need to be applied in order to get reliable results. Similarly, the maximum pulse width jitter limits may be increased in order to accommodate the longer channel.

Table 4-28~~29~~: System Board Transmitter Path Uncorrelated Pulse Width Jitter Requirements at 168.0 GT/s~~Hz~~

Parameter	Min	Max	Unit	Comments
$T_{TX-UPW-TJ}$	0	TBD	ps PP @ BER 10^{-12}	Notes 1, 2, 3
$T_{TX-UPW-DJDD}$	0	TBD	ps PP @ BER 10^{-12}	Notes 1, 2, 3

Notes:
1. PWJ parameters shall be measured after DDJ separation.
2. Measured with optimized preset value.
3. Appropriate CTLE Rx equalization will be applied to allow reliable measurement of pulse width jitter.

Formatted: Font color: Black
Formatted: Font color: Black
Formatted: TableTitle, Don't keep with next
Formatted: Font color: Black
Formatted: Font color: Black
Formatted: Indent: Hanging: 0.81", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 1" + Tab after: 1.25" + Indent at: 1.25", Tab stops: 1.31", Left
Formatted: Indent: Left: 0.44", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 1" + Tab after: 1.25" + Indent at: 1.25"
Formatted: Indent: Hanging: 0.81", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 1" + Tab after: 1.25" + Indent at: 1.25"

~~4.8.13.~~4.8.17. System Board Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

The minimum sensitivity values for the system board's Receiver path compliance at 2.5 GT/s are defined in Table 4-29~~Table 4-30~~Table 4-20 and Table 4-30~~Table 4-31~~Table 4-21. A representative eye diagram is shown in Figure 4-17~~Figure 4-17~~Figure 4-15.

Table 4-29~~30~~4-20: System Board Minimum Receiver Path Sensitivity Requirements at 2.5 GT/s

Parameter	Min	Max	Unit	Comments
V_{RXS}	445	1200	mV	Notes 1, 2, 5
V_{RXS_d}	312	1200	mV	Notes 1, 2, 5
T_{RXS}	287		ps	Notes 1, 3, 5
$J_{RXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	56.5		ps	Notes 1, 4, 5

Notes:

1. An ideal reference clock without jitter is assumed for this specification. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. T_{RXS} is the eye width. The sample size for this measurement is 10^6 UI. This value can be reduced to 274 ps for simulation purpose at BER 10^{-12}.
4. $J_{RXS\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ is the maximum median-to-peak jitter outlier as defined in *the PCI Express Base Specification~~, Revision 4.0~~*. The sample size for this measurement is 10^6 UI. This value can be increased to 63 ps for simulation purpose at BER 10^{-12}.
5. The values in Table 4-29~~Table 4-30~~Table 4-20 are referenced to an ideal 100 Ω differential load at the end of 3-inch 85 Ω differential isolated traces behind a standard connector. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall system board Receiver path. The sensitivity requirements are defined and centered with respect to the jitter median. Exact conditions required for verifying compliance while generating this eye diagram are given in the *PHY Electrical Test Considerations for PCI Express Architecture* document.

Formatted: Font: (Default) Arial, 9 pt

Formatted: Font: (Default) Arial, 9 pt

~~4.8.14.~~4.8.18. System Board Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s

Table 4-~~303~~14 ~~21~~: System Board Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s for a Link that Operates with 3.5 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{RXS}	380	1200	mV	Notes 1, 2, 3
V_{RXS_d}	380	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	1.4		ps RMS	
< 1.5 MHz RMS Jitter	3.0		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:
1. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. The values in Table 4-30~~Table 4-31~~Table 4-21 are calibrated with a reference channel consisting of a 5.0 GT/s System Board Test Channel followed by a 5.0 GT/s Add-in Card Test Channel. After reference calibration, the 5.0 GT/s Add-in Card Test Channel is removed and a standard PCI Express edge finger is placed into the PCI Express connector to be tested. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall system board Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the system board are not specified. The values in Table 4-30~~Table 4-31~~Table 4-21 may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst case mismatch that could be present with a real add-in card or the test setup does not provide crosstalk (only a single Lane is tested, etc), the values in Table 4-16~~Table 4-16~~Table 4-12 must be adjusted accordingly.

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt

Table 4-31324-22: System Board Minimum Receiver Path Sensitivity Requirements at 5.0 GT/s for a Link that Operates with 6.0 dB De-emphasis

Parameter	Min	Max	Unit	Comments
V_{RXS}	306	1200	mV	Notes 1, 2, 3
V_{RXS_d}	260	1200	mV	Notes 1, 2, 3
1.5 – 100 MHz RMS Jitter	1.4		ps RMS	
< 1.5 MHz RMS Jitter	3.0		ps RMS	
1.5 – 100 MHz Dj	30		ps PP	
> 100 MHz Dj	27		ps PP	

Notes:

1. All Links are assumed active while generating this eye diagram.
2. Transition and non-transition bits must be distinguished in order to measure compliance against the de-emphasized voltage level (V_{RXS_d}). V_{RXS} and V_{RXS_d} are differential peak-peak output voltages.
3. The values in Table 4-31Table 4-32Table 4-22 are referenced to an ideal 100 Ω differential load behind 3 inches of isolated 85 Ω trace and a standard PCI Express connector. After reference calibration, the reference fixture is removed and a standard PCI Express edge finger is placed into the PCI Express connector to be tested. The resultant values, when provided to the Receiver interconnect path of the system board, allow for a demonstration of compliance of the overall system board Receiver path. The exact setup and methodology for injecting this signal into the Receiver interconnect path of the system board are not specified. The values in Table 4-31Table 4-32Table 4-22 may need to be adjusted based on the exact test setup and methodology. For example, if the impedance of the test setup does not create the worst case mismatch that could be present with a real add-in card or the test setup does not provide crosstalk (only a single Lane is tested, etc.), the values in Table 4-16Table 4-16Table 4-12 must be adjusted accordingly.

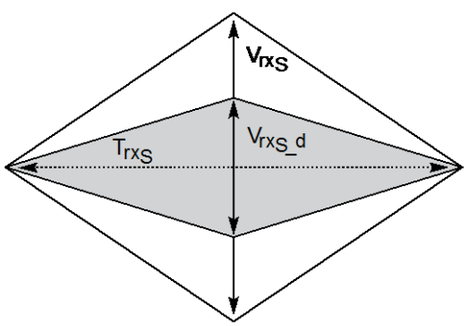


Figure 4-174-17: 5.0 GT/s Representative Composite Eye Diagram for System Board Receiver Path Compliance

Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt
Formatted: Font: (Default) Arial, 9 pt

~~4.8.15.~~4.8.19. System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

The minimum sensitivity values for the system board Receiver path compliance at 8.0 GT/s are defined in Table 4-32~~Table 4-33~~Table 4-23. The receiver path shall be tested with a worst case eye in order to verify that it achieves a BER < 10^{-12}. This worst case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

~~Note:~~ If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

~~Note:~~ If the test is not run in a way that produces the worst case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its equalization settings is tested by applying a signal whose equalization settings are sub-optimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. ~~Note that i~~If the RX under test is more capable than the reference (CTLE+DFE) receiver, the RX may not require the TX to change its equalization levels to achieve a BER < 10^{-12} . In any case, equalization settings resulting from this procedure shall be used for the above RX test and, if the RX requires the TX equalization to change, such change shall be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification.

Table 4-~~323~~34~~,23~~: System Board Minimum Receiver Path Sensitivity Requirements at 8.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX\text{-}EH\text{-}8G}$ Eye height	34	34	mV	Notes 1, 2, 4
$T_{RX\text{-}EH\text{-}8G}$ Eye width	.33	.38	UI	Notes 1, 2
Rj (Random Jitter)	3		ps RMS	Notes 5, 6
Sj (Sinusoidal Jitter) 100 MHz	12.5		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	14		mV PP	Note 3

Notes:

1. The system board reference clock is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are in reference to BER = 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of an 8.0 GT/s System Board Test Channel followed by an 8.0 GT/s Add-in Card Test Channel at the TX SMP connectors on the Add-in Card Test Channel. The calibration is done with the same post processing as the Add-in Card 8.0 GT/s TX test.

Formatted: Not Highlight

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Font color: Black

Formatted: Space Before: 12 pt

Formatted: Font color: Black

After reference calibration, the 8.0 GT/s Add-in Card Test Channel is removed and the System Board Test Channel is connected to the System Board to be tested.

3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at 3.0 ps RMS, it may be adjusted to meet the value for $T_{RX-EH-8G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.

~~4.8.16.~~4.8.20. System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

The minimum sensitivity values for the system board Receiver path compliance at 16.0 GT/s are defined in Table 4-33~~Table 4-34~~ ~~Table 4-23~~. The receiver path shall be tested with a worst case eye in order to verify that it achieves a BER < 10^{-12}. This worst case eye is calibrated using TX equalization settings that are optimal with the reference equalizer for the calibration channel. After calibration, the test-generator's equalization settings may be adjusted using the transmitter equalization setting in the required TX equalization space preferred by the device under test, without changing any other parameter of the test signal or recalibrating the test signal.

~~Note:~~ If the test generator's TX equalization settings are adjusted away from the optimal settings and the test generator is not able to change transmitter equalization without impacting other calibrated parameters – then the other parameters must be adjusted back to the specified values.

~~Note:~~ If the test is not run in a way that produces the worst case cross-talk that would be present with all lanes active, the additional cross-talk must be accounted for in some other way.

While the receiver's capacity to adapt its own equalization is part of the test described above, its ability to request the link partner's transmitter to change its equalization settings is tested by applying a signal whose equalization settings are sub-optimal compared to the jitter sensitivity test signal described above. For this signal, the reference receiver would not be able to achieve proper equalization by means of its own CTLE and DFE alone. Such a signal can be defined using the signal resulting from the calibration method described above and adjusting the test-generator equalization. ~~Note that i~~If the RX under test is more capable than the reference (CTLE+DFE) receiver, the RX may not require the TX to change its equalization levels to achieve a BER < 10^{-12} . In any case, equalization settings resulting from this procedure shall be used for the above RX test and, if the RX requires the TX equalization to change, such change shall be accommodated by the test set-up used.

A specific methodology for this procedure is outside the scope of this specification.

Formatted: Not Highlight

Formatted: Font color: Black

Formatted: TableTitle, Don't suppress line numbers

Table 4-~~33344-23~~: System Board Minimum Receiver Path Sensitivity Requirements at 16.0 GT/s

Parameter	Min	Max	Unit	Comments
$V_{RX\text{-}EH\text{-}168G}$ Eye height	~~TBD~~15	~~TBD~~15	mV	Notes 1, 2, 4
$T_{RX\text{-}EH\text{-}168G}$ Eye width	~~TBD~~0.3	~~TBD~~0.3	UI	Notes 1, 2
Rj (Random Jitter)	TBD		ps RMS	Notes 5, 6
Sj (Sinusoidal Jitter) 100 MHz	TBD		ps PP	Note 6
Differential Mode Sinusoidal Interference 2.1 GHz	TBD		mV PP	Note 3

Notes:

1. The system board reference clock is assumed for this specification. The 128/130b compliance pattern must be used during calibration for this test. Modified compliance pattern is used when the receiver test is run. Eye height and width values are in reference to BER = 10^{-12}.
2. The values in this table are initially calibrated with a reference channel consisting of a TBD System Board Test Channel followed by a TBD Add-in Card Test Channel at the TX SMP connectors on the Add-in Card Test Channel. The calibration is done with the same post processing as the Add-in Card 16.0 GT/s TX test. After reference calibration, the 16.0 GT/s Add-in Card Test Channel is removed and the System Board Test Channel is connected to the System Board to be tested.
3. Eye height and width are specified after the application of the reference receiver. When the optimization of the reference receiver's CTLE and DFE yields an eye height and/or eye width larger than specified, the value for DM-interference is increased.
4. Eye height limits do not account for limitations in test equipment voltage resolution.
5. Rj is applied over the following range. The low frequency limit may be between 1.5 and 10 MHz, and the upper limit is 1.0 GHz. While the nominal value is specified at TBD RMS, it may be adjusted to meet the value for $T_{RX\text{-}EH\text{-}168G}$ Eye Width.
6. Rj and Sj are measured without post-processing filters.

~~5.~~

Formatted: Font color: Black

Formatted: Highlight

Formatted: Indent: Left: 0.25", No bullets or numbering

5

5. 150 W, 225 W, and 300 W Add-in Card Power

A PCI Express 150 W ~~ATX~~ add-in card must adhere to strict power distribution, power-up, and power consumption requirements to ensure robust operation. Power may only be drawn using two techniques: the standard PCI Express connector and the dedicated 150 W ~~ATX~~ power connector defined in this specification.

It is necessary for a PCI Express 150 W add-in card to be seamlessly integrated with a 150 W-capable system to ensure interoperability. To that end, it is required that the ~~150~~ 150 W add-in card be properly powered in the system. To guarantee proper operation and provide a safe user experience, the following power delivery requirements must be adhered to by a PCI Express 150 W add-in card:

- The +~~12~~ 12 V delivered from the standard connector and the additional +~~12~~ 12 V delivered via the dedicated 2 x 3 power supply connector must be treated as coming from two separate system power supply rails.
- The two +12 V input potentials must not be electrically shorted at any point on a PCI Express 150 W add-in card.
- No specific power sequencing between the slot and 2 x 3 connector power can be assumed. A PCI Express 150 W add-in card must handle all possible combinations.

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

IMPLEMENTATION NOTE !!!

Safety Certifications

PCI Express 150 W add-in cards and capable systems must adhere to all applicable safety certifications (e.g., UL 240 VA) at all times.

A PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card must adhere to strict power distribution, power-up, and power consumption requirements to ensure robust operation. Power must only be drawn using the three specified connectors: the standard PCI Express connector, the 2 x 4 auxiliary power connector, and the 2 x 3 auxiliary power connector as defined in this specification.

It is necessary for a PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card to be seamlessly integrated with a 225 W/~~300~~ 300 W capable system to ensure interoperability. To that end, it is required that the card be properly powered in the system. To guarantee proper operation and provide a safe user experience, the following power delivery requirements must be adhered to by a PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card:

- The +~~12~~ 12 V delivered from the standard edge connector and the additional +~~12~~ 12 V~~(s)~~ delivered via the dedicated 2 x 3 and/or 2 x 4 auxiliary power connector(s) must be treated as coming from independent separate system power supply rails.
- The different +~~12~~ 12 V input potentials from different connectors must not be electrically shorted at any point on a PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card.
- The power pins of a single 2 x 3 or 2 x 4 auxiliary power connector can be shorted together.
- No specific power sequencing between the slot, the 2 x 3 connector, and the 2 x 4 connector power can be assumed. A PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card must handle all possible combinations.
- A 300 W add-in card can receive power by the following methods: 10
  - 75 W from the PCI Express connector plus 150 W from a 2 x 4 connector plus 75 W from a 2 x 3 connector.
  - 75 W from the PCI Express connector plus 75 W from a first 2 x 3 connector, plus 75 W from a second 2 x 3 connector, plus 75 W from a third 2 x 3 connector. Note that this is NOT the preferred approach.

- ~~A 300 300 W add-in card can receive power by the following methods:~~
  - ~~75 It is recommended that 75 W be taken from the PCI Express connector plus 150 150 W from a 2 x 4 connector plus 75 75 W from a 2 x 3 connector.~~
  - ~~75 It is permitted but not recommended that 75 W be taken from the PCI Express connector plus 75 75 W from a first 2 x 3 connector, plus 75 W from a second 2 x 3 connector, plus 75 75 W from a third 2 x 3 connector. Note that this is NOT the preferred approach.~~

- A ~~225~~ 225 W add-in card can receive power by one of the following methods:
  - ~~75~~ 75 W from the PCI Express connector plus ~~150~~ 150 W from a 2 x 4 connector.
  - ~~75~~ 75 W from the PCI Express connector plus ~~75~~ 75 W from a 2 x 4 connector plus ~~75~~ 75 W from a 2 x 3 connector.
  - ~~75~~ 75 W from the PCI Express connector plus ~~75~~ 75 W from a first 2 x 3 connector plus ~~75~~ 75 W from a second 2 x 3 connector.

IMPLEMENTATION NOTE

Auxiliary Power Connector Configurations for ~~225~~ 225 W / ~~300~~ 300 W Add-in Cards

PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in cards have a wide variety of power delivery configurations to choose from. This flexibility will lower the cost of migration as certain existing components (e.g., power supply units) can be reused.

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Font: 12 pt

Formatted: Font: (Default) Garamond, 12 pt, Font color: Black

Formatted: Bulleted List, Indent: Left: 0", Hanging: 0.19", Space After: 0 pt

Formatted: No bullets or numbering

Formatted: Highlight

Commented [NM10]: Delete the note?

Formatted: Highlight

Formatted: Highlight

Formatted: Indent: Left: 0.19", No bullets or numbering

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Highlight

Formatted: Left

Formatted: Font: Arial Black

Formatted: Font: 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt

Formatted: Space After: 0.6 line

~~Safety Certifications~~

~~PCI Express 225 W/300 W add-in cards and capable systems must adhere to all applicable safety certifications (e.g., UL 240 VA) at all times.~~

- PCI Express 225 W / 300 W add-in cards and capable systems must adhere to all applicable safety certifications (e.g., UL 240 VA) at all times

Formatted: Font: 10 pt

Formatted: Space Before: 0 pt, After: 0.6 line

Formatted: Space After: 0.6 line

Formatted: Body Text, Suppress line numbers

Formatted: Style Bullet box + Black, Indent: Left: 0", Hanging: 0.13"

5.1. ~~150~~ 150 W Add-in Card Power-Up Sequencing

The following specified power-up sequencing process permits a PCI Express 150 W add-in card to sense if the PCI Express 150 W connector is plugged in and then initially draw up to a maximum of 75 W. This methodology allows a PCI Express 150 W add-in card to circumvent the 25 W maximum power consumption that is required for all add-in cards prior to being enabled for higher power consumption via a Slot Power Limit message.

The system power-up sequencing follows the Slot Power Limit Control mechanism as defined in Chapter 6 of the *PCI Express Base Specification*~~, Revision 4.0~~. An overview of power-up sequencing is shown in Figure 5-1~~Figure 5-1~~~~Figure 5-1~~.

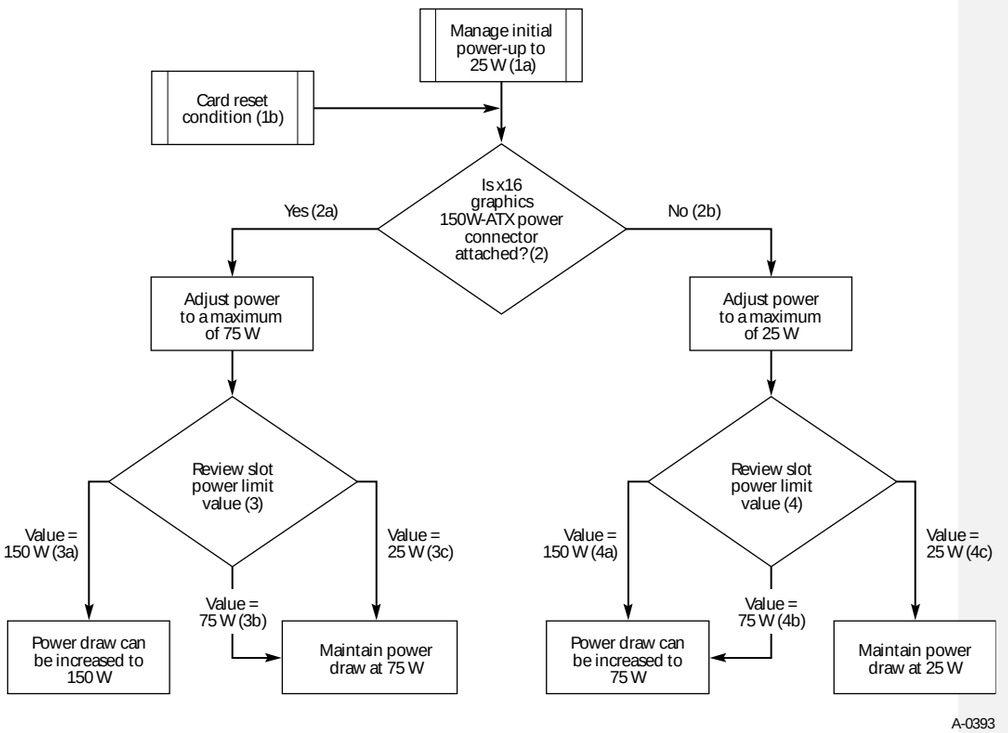


Figure 5-~~15-1~~: PCI Express ~~150~~ 150 W Add-in Card Power-Up Sequence

1. Initial power-up or reset condition.
   a. At initial power-up, manage maximum power to <= ~~25~~ 25 W maximum for sensing of the PCI Express 150 W~~-ATX~~ power connector.
   b. An add-in card cannot remember a previous power limit setting through a reset. A card that has been reset must start the process over again as with initial power application. (Total power in this state will be dependent on the Slot Power Limit Value prior to the reset.)
2. Detect if a PCI Express 150 W~~-ATX~~ power connector is plugged into the add-in card using the allocated Sense pin.
   a. Yes. If the connector is installed, then the PCI Express 150 W~~-ATX~~ add-in card can be adjusted to a combined maximum of ~~75~~ 75 W of power using the PCI Express 150 W~~-ATX~~ power connector and the CEM connector. In this situation, a maximum of 25 W can be drawn from the connector. Proceed to step 3.
   b. No. If the PCI Express 150 W~~-ATX~~ power cable is not connected, then power consumption must be adjusted to a maximum of ~~25~~ 25 W. Proceed to step 4.
3. Review Slot Power Limit Value. PCI Express 150 W~~-ATX~~ power connector was sensed.
   a. Value = ~~150~~ 150 W. If the received slot power message indicates ~~150~~ 150 W, a PCI Express 150 W~~-ATX~~ add-in card can proceed to draw up to a maximum of ~~150~~ 150 W. This is a total of ~~75~~ 75 W from the PCI Express connector and ~~75~~ 75 W via the dedicated PCI Express 150 W~~-ATX~~ power connector.
   b. Value = ~~75~~ 75 W. If the received slot power message indicates ~~75~~ 75 W, power consumption must be maintained at a combined maximum of ~~75~~ 75 W of power using the PCI Express x16 150 W~~-ATX~~ power connector and the connector. In this situation, a maximum of ~~25~~ 25 W can be drawn from the connector.
   c. Value = ~~25~~ 25 W. If the received slot power message indicates ~~25~~ 25 W or if no slot power message is received, then power consumption must be maintained at a combined maximum of ~~75~~ 75 W of power using the PCI Express 150 W~~-ATX~~ power connector and the connector. In this situation, a maximum of ~~25~~ 25 W can draw from the connector.
4. Review Slot Power Limit Value. PCI Express 150 W~~-ATX~~ power connector was not sensed.
   a. Value = ~~150~~ 150 W. If the received slot power message indicates ~~150~~ 150 W, power consumption can be increased to a maximum of ~~75~~ 75 W via power from the connector.
   b. Value = ~~75~~ 75 W. If the received slot power message indicates ~~75~~ 75 W, power consumption can be increased to a maximum of ~~75~~ 75 W via power from the connector.
   c. Value = ~~25~~ 25 W. If the received slot power message indicates ~~25~~ 25 W or if no slot power message is received, total ~~graphics~~ power must be managed to a maximum of ~~25~~ 25 W at all times.

~~-~~IMPLEMENTATION NOTE

Power-up Sequencing Configuration Issues

Steps 3b, 3c, 4a, 4b, and 4c above are configurations in the power-up sequencing for a PCI Express 150 W~~-ATX~~ add-in card that result in less than the full ~~150~~ 150 W of power being available to the add-in card. Any operation such as actual display to a connected output device, whether VGA or otherwise, at less than ~~150~~ 150 W is not guaranteed and is implementation dependent. However, it is preferred that at least an implementation supplied warning text message is displayed to alert the user of the configuration issue.

Formatted: Font: Arial Black

Formatted: Font: Arial Black

Formatted: Font: 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt

Formatted: Space After: 3 pt

Power Distribution and Consumption

PCI Express 150 W add-in cards must follow a stringent set of rules for power distribution to the card and power consumption of the card. Drawing power from the system in any way that is not specified is not allowed as is consuming power above the maximum of ~~150~~ 150 W.

Formatted: Font: 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt

Formatted: Space After: 3 pt

5.2. ~~225~~ 225 W and ~~300~~ 300 W Add-in Card Power-Up Sequencing

The following specified power-up sequencing process permits a PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card to sense if the auxiliary connectors are plugged in and identify the initial power draw limit. This methodology allows a PCI Express ~~225~~ 225 W/~~300~~ 300 W add-in card to circumvent the ~~25~~ 25 W maximum power consumption that is required in this specification for a add-in card prior to being enabled for higher power consumption via a Slot Power Limit message.

The system power-up sequencing follows the Slot Power Limit Control mechanism as defined in Chapter 6 of the *PCI Express Base Specification*~~, Revision 4.0~~. The power-up sequencing for a 225 W/300 W card is as follows:

Immediately after system reset and before the card has determined which supplemental power connectors are attached, the card power is limited to ~~25~~ 25 W which must be drawn from the PCI Express slot.

At system power up, the permitted initial power draw depends on the auxiliary power connector configurations on the card and how many sense pins are detected. Table 5-1~~Table 5-1~~~~Table 5-1~~ to Table 5-5~~Table 5-5~~~~Table 5-5~~ enumerate the different possibilities.

After system reset is released and the PCI Express Link is up, the card will receive the Slot_Power_Limit message.

- If the Slot_Power_Limit is bigger than or equal to the permitted initial power draw, the card can then draw power up to the Slot_Power_Limit in any order from the PCI Express edge connector, the 2 x 3 connector (if it exists), and the 2 x 4 connector (if it exists), subject to and limited to the individual power ratings of the respective connectors.
- If the Slot_Power_Limit is smaller than the permitted initial power draw, the card can ignore the Slot_Power_Limit message and continue to draw the same amount of power as permitted at system power up time.

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Table 5-~~15-1~~: PCI Express ~~300~~ 300 W Card (with One 2 x 4 and One 2 x 3 Connector) Permitted Initial Power Draw

2 x 4 Sense0 Detected?	2 x 4 Sense1 Detected?	2 x 3 Sense Detected?	Power Draw Permitted at System Power Up
N	N	N	~~25~~ 25 W available from PCI Express edge connector
N	N	Y	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector
Y	N	N	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 4 connector
Y	N	Y	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector ~~50~~ 50 W available from 2 x 4 connector
Y	Y	N	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~100~~ 100 W available from 2 x 4 connector
Y	Y	Y	Total of ~~175~~ 175 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~100~~ 100 W available from 2 x 4 connector ~~50~~ 50 W available from 2 x 3 connector

Table 5-~~25-2~~: PCI Express 300 W Card (with Three 2 x 3 Connectors) Permitted Initial Power Draw

First 2 x 3 Sense Detected?	Second 2 x 3 Sense Detected?	Third 2 x 3 Sense Detected?	Power Draw Permitted at System Power Up
N	N	N	~~25~~ 25 W available from PCI Express edge connector
N	N	Y	Total of ~~75~~ 75 W is available: 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector
N	Y	N	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector
Y	N	N	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector

First 2 x 3 Sense Detected?	Second 2 x 3 Sense Detected?	Third 2 x 3 Sense Detected?	Power Draw Permitted at System Power Up
Y	N	Y	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from the first 2 x 3 connector ~~50~~ 50 W available from the third 2 x 3 connector
Y	Y	N	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from the first 2 x 3 connector ~~50~~ 50 W available from the second 2 x 3 connector
N	Y	Y	Total of 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from the second 2 x 3 connector ~~50~~ 50 W available from the third 2 x 3 connector
Y	Y	Y	Total of ~~175~~ 175 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from the first 2 x 3 connector ~~50~~ 50 W available from the second 2 x 3 connector ~~50~~ 50 W available from the third 2 x 3 connector

Table 5-~~3~~5-~~3~~: PCI Express ~~225~~ 225 W Card (with One 2 x 4 Connector) Permitted Initial Power Draw

2 x 4 Sense0 Detected?	2 x 4 Sense1 Detected?	Power Draw Permitted at System Power Up
N	N	~~25~~ 25 W available from PCI Express edge connector
Y	N	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 4 connector
Y	Y	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~100~~ 100 W available from 2 x 4 connector

Table 5-~~45~~ 4: PCI Express ~~225~~ 225 W Card (with Two 2 x 3 Connectors) Permitted Initial Power Draw

First 2 x 3 Sense Detected?	Second 2 x 3 Sense Detected?	Power Draw Permitted at System Power Up
N	N	~~25~~ 25 W available from PCI Express edge connector
N	Y	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from second 2 x 3 connector
Y	N	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from first 2 x 3 connector
Y	Y	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from first 2 x 3 connector ~~50~~ 50 W available from second 2 x 3 connector

Table 5-~~55~~ 5: PCI Express ~~225~~ 225 W Card (with One 2 x 3 and One 2 x 4 Connector) Permitted Initial Power Draw

2 x 4 Sense0 Detected?	2 x 4 Sense1 Detected?	2 x 3 Sense Detected?	Power Draw Permitted at System Power Up
N	N	N	~~25~~ 25 W available from PCI Express edge connector
N	N	Y	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector
Y	N	N	Total of ~~75~~ 75 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 4 connector
Y	N	Y	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~50~~ 50 W available from 2 x 3 connector ~~50~~ 50 W available from 2 x 4 connector
Y	Y	N	Total of ~~125~~ 125 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~100~~ 100 W available from 2 x 4 connector
Y	Y	Y	Total of ~~175~~ 175 W is available: ~~25~~ 25 W available from PCI Express edge connector ~~100~~ 100 W available from 2 x 4 connector ~~50~~ 50 W available from 2 x 3 connector

For a ~~225~~ 225 W/~~300~~ 300 W add-in card, if the auxiliary power connector(s) is not populated in such a way that results in the full ~~225~~ 225 W/~~300~~ 300 W power being available to the graphics add-in card, any graphics operation and actual display to a connected output device, whether VGA or otherwise, is not guaranteed and is implementation dependent. However, it is preferred that an implementation supplied warning text message is displayed to alert the user of the configuration issue.

6

6. Card Connector Specification

A family of PCI Express vertical edge card connectors supports x1, x4, x8, and x16 Link widths to suit different bandwidth requirements. These connectors support the PCI Express signal and power requirements, as well as auxiliary signals used to facilitate the interface between system board and add-in card hardware. This chapter defines the connector mating interfaces and footprints, as well as the electrical, mechanical, and environmental requirements.

6.1. Connector Pinout

Table 6-1~~Table 6-1~~~~Table 6-1~~ shows the pinout definition for the x1, x4, x8, and x16 PCI Express connectors.
The auxiliary pins are identified in the shaded areas.

Table 6-~~16-1~~: PCI Express Connectors Pinout

Pin#		Side B	Side A	
	Name	**Description**	**Name**	**Description**
1	+12V	+12 V power	PRSNT1#	Hot-Plug presence detect
2	+12V	+12 V power	+12V	+12 V power
3	+12V	+12 V power	+12V	+12 V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus (System Management Bus) clock	JTAG2	TCK (Test Clock), clock input for JTAG interface
6	SMDAT	SMBus (System Management Bus) data	JTAG3	TDI (Test Data Input)
7	GND	Ground	JTAG4	TDO (Test Data Output)
8	+3.3V	+3.3 V power	JTAG5	TMS (Test Mode Select)
9	JTAG1	TRST# (Test Reset) resets the JTAG interface	+3.3V	+3.3 V power
10	+3.3Vaux	+3.3 V auxiliary power	+3.3V	+3.3 V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental reset
Mechanical key				
12	CLKREQ#	Clock Request Signal	GND	Ground
13	GND	Ground	REFCLK+	Reference clock (differential pair)
14	PETp0	Transmitter differential pair, Lane 0	REFCLK-	
15	PETn0		GND	Ground
16	GND	Ground	PERp0	Receiver differential pair, Lane 0
17	PRSNT2#	Hot-Plug presence detect	PERn0	
18	GND	Ground	GND	Ground
End of the x1 connector				
19	PETp1	Transmitter differential pair,	RSVD	

Pin#		Side B	Side A	
	Name	**Description**	**Name**	**Description**
20	PETn1	Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential pair, Lane 1
22	GND	Ground	PERn1	
23	PETp2	Transmitter differential pair,	GND	Ground
24	PETn2	Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential pair, Lane 2
26	GND	Ground	PERn2	
27	PETp3	Transmitter differential pair,	GND	Ground
28	PETn3	Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential pair, Lane 3
30	~~RSVD~~PWRBRK#	~~Power Break Signal~~Emergency Power Reduction	PERn3	
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
End of the x4 connector				
33	PETp4	Transmitter differential pair,	RSVD	Reserved
34	PETn4	Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential pair, Lane 4
36	GND	Ground	PERn4	
37	PETp5	Transmitter differential pair,	GND	Ground
38	PETn5	Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential pair, Lane 5
40	GND	Ground	PERn5	
41	PETp6	Transmitter differential pair,	GND	Ground
42	PETn6	Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential pair, Lane 6
44	GND	Ground	PERn6	
45	PETp7	Transmitter differential pair,	GND	Ground
46	PETn7	Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential pair, Lane 7
48	PRSNT2#	Hot-Plug presence detect	PERn7	
49	GND	Ground	GND	Ground
End of the x8 connector				
50	PETp8	Transmitter differential pair,	RSVD	Reserved
51	PETn8	Lane 8	GND	Ground
52	GND	Ground	PERp8	Receiver differential pair, Lane 8
53	GND	Ground	PERn8	
54	PETp9	Transmitter differential pair,	GND	Ground
55	PETn9	Lane 9	GND	Ground
56	GND	Ground	PERp9	Receiver differential pair, Lane 9
57	GND	Ground	PERn9	
58	PETp10	Transmitter differential pair,	GND	Ground
59	PETn10	Lane 10	GND	Ground
60	GND	Ground	PERp10	Receiver differential pair, Lane 10
61	GND	Ground	PERn10	
62	PETp11	Transmitter differential pair,	GND	Ground
63	PETn11	Lane 11	GND	Ground
64	GND	Ground	PERp11	Receiver differential pair, Lane 11
65	GND	Ground	PERn11	
66	PETp12	Transmitter differential pair,	GND	Ground
67	PETn12	Lane 12	GND	Ground
68	GND	Ground	PERp12	Receiver differential pair, Lane 12
69	GND	Ground	PERn12	

Pin#		Side B	Side A	
	Name	**Description**	**Name**	**Description**
70	PETp13	Transmitter differential pair, Lane 13	GND	Ground
71	PETn13		GND	Ground
72	GND	Ground	PERp13	Receiver differential pair, Lane 13
73	GND	Ground	PERn13	
74	PETp14	Transmitter differential pair, Lane 14	GND	Ground
75	PETn14		GND	Ground
76	GND	Ground	PERp14	Receiver differential pair, Lane 14
77	GND	Ground	PERn14	
78	PETp15	Transmitter differential pair, Lane 15	GND	Ground
79	PETn15		GND	Ground
80	GND	Ground	PERp15	Receiver differential pair, Lane 15
81	PRSNT2#	Hot-Plug presence detect	PERn15	
82	RSVD	Reserved	GND	Ground
End of the x16 connector				

~~The~~ Be aware of the following points ~~should be noted~~:

- The pins are numbered as shown in Figure 6-2~~Figure 6-2~~~~Figure 6-2~~ in ascending order from the left to the right, with side A on the top of the centerline and side B on the bottom of the centerline.
- The PCI Express interface pins PETpx, PETnx, PERpx, and PERnx are named with the following convention: "PE" stands for PCI Express *high speed*, "T" for *Transmitter*, "R" for *Receiver*, "p" for *positive* (+), and "n" for *negative* (-).
- By default, PETpx and PETnx pins (the Transmitter differential pair of the connector) shall be connected to the PCI Express Transmitter differential pair on the system board, and to the PCI Express Receiver differential pair on the add-in card.
- By default, PERpx and PERnx pins (the Receiver differential pair of the connector) shall be connected to the PCI Express Receiver differential pair on the system board, and to the PCI Express Transmitter differential pair on the add-in card.
- However, the "p" and "n" connections may be reversed to simplify PCB trace routing and minimize vias if needed. All PCI-Express Receivers incorporate automatic Lane Polarity Inversion as part of the Link Initialization and Training and will correct the polarity independently on each Lane. Refer to the *PCI Express Base Specification*~~, Revision 4.0~~.
- If the component on the system board or add-in card does not support the optional PCI Express Lane Reversal functions, they must connect each Transmitter and Receiver Lane to the add-in card connector lanes as shown in Table 6-1~~Table 6-1~~~~Table 6-1~~. For example, a x4 component must connect Lane 0 to 0, Lane 1 to 1, Lane 2 to 2, and Lane 3 to 3.
- If the component on the system board or add-in card supports the optional PCI Express Lane Reversal function, it may connect each Transmitter and Receiver Lane to the add-in card connector lanes as shown in Table 6-1~~Table 6-1~~~~Table 6-1~~ or it may connect the Transmitter and Receiver lanes using a reversed Lane ordering. Either Lane ordering may be used to simplify PCB trace routing and minimize vias. However, the transmitting and receiving lanes must be connected with the same Lane ordering. For example, a x4 component may connect Lane 0 to 0,

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Lane 1 to 1, Lane 2 to 2, and Lane 3 to 3 or it may connect Lane 0 to 3, Lane 1 to 2, Lane 2 to 1, and Lane 3 to 0.

- The connectors and the add-in cards are keyed such that smaller add-in cards can be put in larger connectors. For example, a x1 card can be inserted into the x4, x8, and x16 connectors. This is referred to as up-plugging.
- Adjacent differential pairs are separated by two ground pins to manage the connector crosstalk.
- See Chapter 2 for auxiliary signals description and implementation, except the +3.3Vaux and PRSNT1# and PRSNT2# pins. The requirements for +3.3Vaux are discussed in Chapter 4 and presence detect is discussed in Chapter 3.
- PRSNT1# and PRSNT2# pins are for card presence detect. One present detect pin at each end of a connector guarantees that at least one of the present detect pins is last-mate/first-break. More than two PRSNT2# pins in the x4, x8, and x16 PCI Express connectors are for the purpose of supporting up-plugging. See Chapter 3 for detailed discussions on presence detect.
- The sequential mating for Hot-Plug is accomplished by staggering the ~~edge-finger~~edge-fingers on the add-in card, as shown in Section 6.2. Detailed requirements on Hot-Plug are covered in Chapter 3.
- Power pins (+3.3-V, +3.3Vaux, and +12-V) are defined based on the PCI Express power delivery requirements specified in Chapter 4, with the connector contact carrying capability being 1.1 A per pin. The power that goes through the connector shall not exceed the maximum power specified for a given add-in card size, as defined in Section 4.2.

6.2. Connector Interface Definitions

The PCI Express through hole connector outline~~,~~ and footprint~~, and the corresponding add-in card edge-finger dimensions~~ are shown in Figure 6-1~~Figure 6-1~~Figure 6-1, and ~~Figure 6-2~~Figure 6-2Figure 6-2~~, and Figure 6-3~~and T~~the surface mount connector outline and footprint are shown in Figure 6-3 and Figure 6-4. The ~~corresponding~~ add-in card edge-finger dimensions are shown in Figure 6-5. The add-in card edge-finger dimensions apply to both types of connectors.

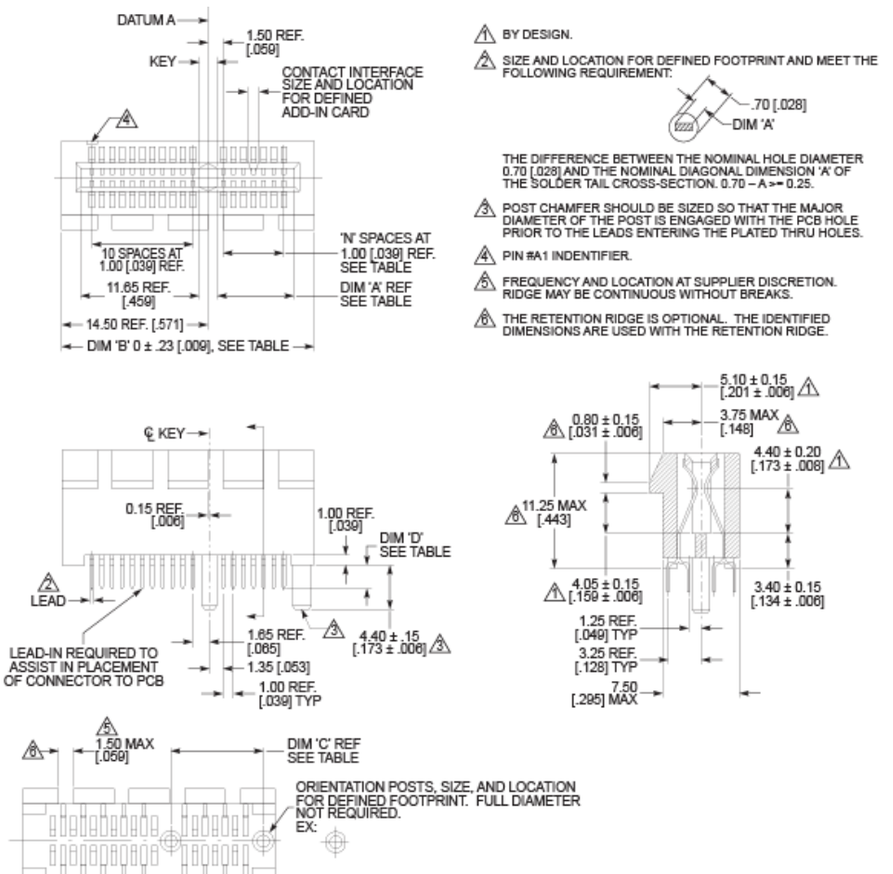
Formatted: Font color: Auto

Formatted: Do not check spelling or grammar

Formatted: Font color: Auto

Formatted: Font color: Auto

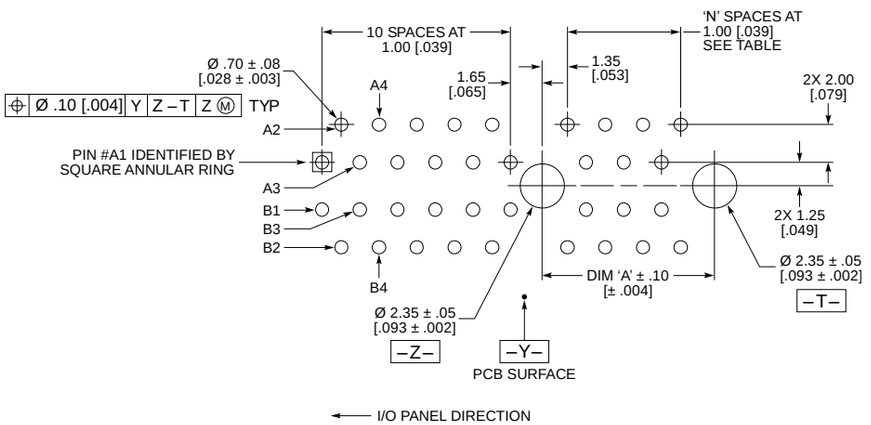
Formatted: Highlight



CONNECTOR LINK WIDTH	# POS REF	N	DIM 'A'	DIM 'B'	DIM 'C'	PCB THK (REF)	DIM 'D'
X1	36	6	7.65 [.301]	25.00 [.984]	9.15 [.360]	1.58 [.062]	2.30 +.25/–.13 [.091 +.010/–.005]
X4	64	20	21.65 [.852]	39.00 [1.535]	23.15 [.911]		
X8	98	37	38.65 [1.522]	56.00 [2.205]	40.15 [1.581]	2.36 [.093]	3.10 +.25/–.13 [.122 +.010/–.005]
X16	164	70	71.65 [2.821]	89.00 [3.504]	73.15 [2.880]		

A-0899a

Figure 6-~~16-1~~: ~~Recommended~~ Through Hole Mount Connector Outline~~Form Factor~~



CONNECTOR LINK WIDTH	# POS REF	N	DIM 'A'
X1	36	6	9.15 [.360]
X4	64	20	23.15 [.911]
X8	98	37	40.15 [1.581]
X16	164	70	73.15 [2.880]

A-0900

Figure 6-~~26-2~~: Recommended Through Hole Mount Connector Footprint

Formatted: figure

Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Font color: Auto

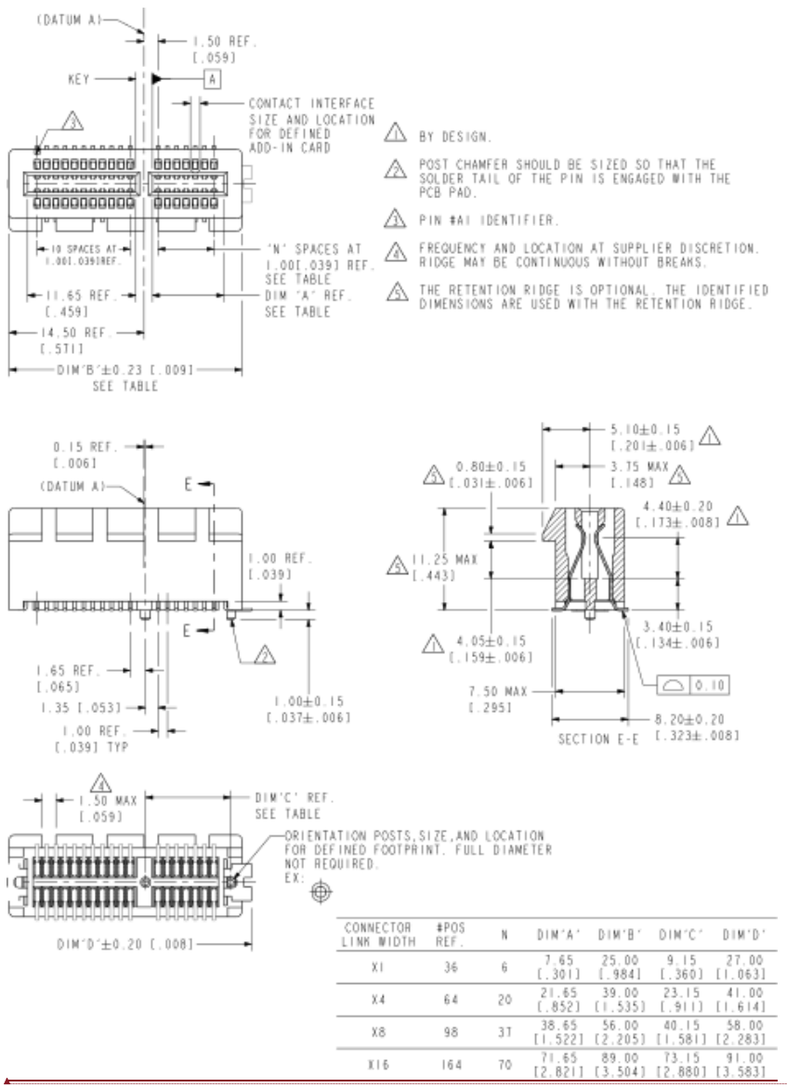
Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Font color: Auto

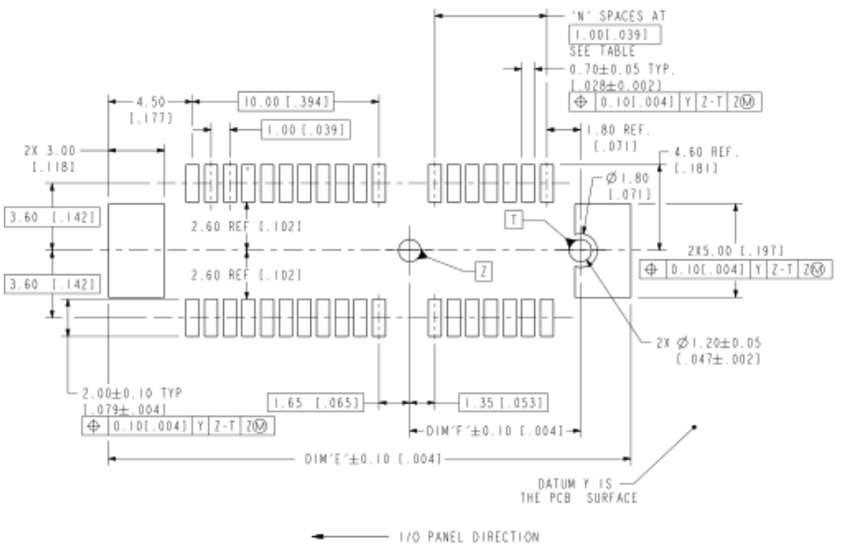


CONNECTOR LINK WIDTH	#POS REF.	N	DIM 'A'	DIM 'B'	DIM 'C'	DIM 'D'
X1	36	6	7.65 [.301]	25.00 [.984]	9.15 [.360]	27.00 [1.063]
X4	64	20	21.65 [.852]	39.00 [1.535]	23.15 [.911]	41.00 [1.614]
X8	98	37	38.65 [1.522]	56.00 [2.205]	40.15 [1.581]	58.00 [2.283]
X16	164	70	71.65 [2.821]	89.00 [3.504]	73.15 [2.880]	91.00 [3.583]

Figure 6-3: ~~Recommended~~ Surfact Mount Connector ~~Form Factor~~ Outline

Formatted: Check spelling and grammar

Formatted: figure, Don't keep with next



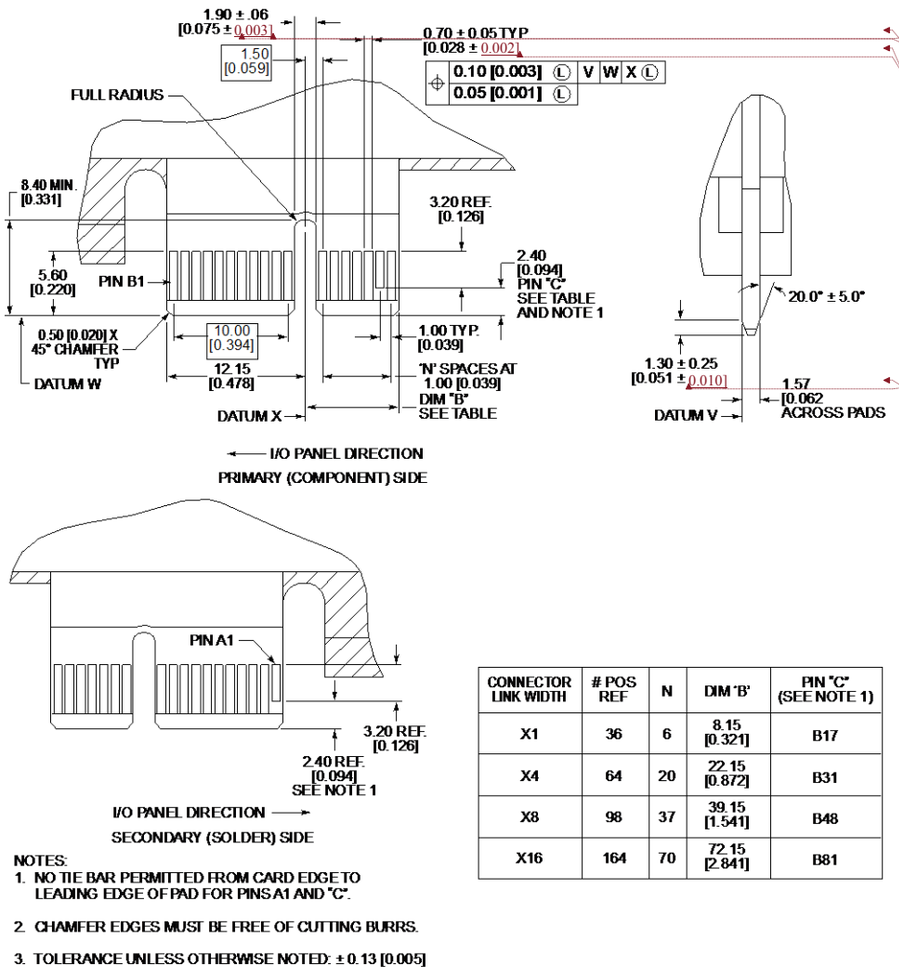
CONNECTOR LINK WIDTH	#POS REF.	N	DIM'E'	DIM'F'
X1	36	6	28.00 [1.102]	9.15 [.360]
X4	64	20	42.00 [1.654]	23.15 [.911]
X8	98	37	59.00 [2.323]	40.15 [1.581]
X16	164	70	92.00 [3.622]	73.15 [2.880]

NOTE: TOLERANCE UNLESS OTHER NOTED IS ±0.13 [0.005].

Figure 6-4: Recommended Surfact Mount Connector Footprint

Formatted: figure, Space Before: 0 pt, After: 0 pt, Don't keep with next

Formatted: Space Before: 2 pt, After: 12 pt, Don't keep with next



CONNECTOR LINK WIDTH	# POS REF	N	DIM 'B'	PIN "C" (SEE NOTE 1)
X1	36	6	8.15 [0.321]	B17
X4	64	20	22.15 [0.872]	B31
X8	98	37	39.15 [1.541]	B48
X16	164	70	72.15 [2.841]	B81

NOTES:
1. NO TIE BAR PERMITTED FROM CARD EDGE TO LEADING EDGE OF PAD FOR PINS A1 AND "C".
2. CHAMFER EDGES MUST BE FREE OF CUTTING BURRS.
3. TOLERANCE UNLESS OTHERWISE NOTED: ± 0.13 [0.005]

A-0901b

Figure 6-~~56-5~~: Add-in Card Edge-Finger Dimensions

Formatted: Font: 8 pt

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single

~~The~~ Be aware of the following points ~~should be noted~~:

~~TBD update to accommodate both through hole and SMT.~~

- The connector has a 1.~~00~~00 mm contact pitch.
- The contact shall be pre-loaded, similar to the PCI connector.
- The through hole mount connector footprint (Figure 6-2~~Figure 6-2~~Figure 6-2) requires two 2.35 mm diameter location holes, working with either plastic or metal pegs/posts or metal board locks. The two 2.35 mm diameter location holes ~~(shown in Figure 6-2)~~ may either be drilled or plated through holes (PTH). The surface mount technology connector footprint (Figure 6-4~~Error! Reference source not found.~~) requires two 1.20 mm holes, working with either plastic or metal pegs / posts or metal board locks. The two 1.20 mm diameter location holes may either be drilled or plated through holes. Plated through holes enable the soldering of a connector with metal guide posts to provide more secure retention for larger/heavier add-in cards. Metal board locks are also allowed, although Figure 6-1~~Figure 6-1~~Figure 6-1 shows only the plastic pegs on the connector housing.
- Figure 6-5~~Figure 6-5~~Figure 6-3 defines only the mating interface related dimensions. Other add-in card dimensions are defined in Chapter ~~6~~9.
- The PRSNT1# and PRSNT2# pins shown in Figure 6-5~~Figure 6-5~~Figure 6-3 are 1 mm shorter than the other fingers. Those pins are designated as A1, B17, B31, B48, and B81, where applicable. No plating tie bar is allowed underneath the PRSNT1# and PRSNT2# pins because those pins are meant to be last-mate and first-break.
- As shown in Figure 6-1~~Figure 6-1~~ and Figure 6-3, **Error! Reference source not found.** ~~**Error! Reference source not found.**~~Figure 6-1, an optional ridge feature is defined on the top of the connector housing on one side. This feature can be used to facilitate card retention. A retention clip may be mounted on an add-in card and latched on the ridge.
- Two types of add-in cards must be "retention ready":

  – Graphics cards.

  – x1, x4, x8, or x16 I/O cards that, in the judgment of the OEM or card manufacturers, have sufficient weight or length that the card may need an additional retention point for stability.

  Retention ready means that the add-in card manufacturer must have selected (or created) a retention mechanism and made provisions on the card to facilitate the retention mechanism. The reference retention mechanism designs and related component keep-out or height restriction areas are defined in the *PCI Express Graphics Card Thermal Mechanical Design Guidelines*.

  The full-length card, 321.00 mm (12.283 inches) long, is considered retention ready. The mounting holes on one end of the full-length card allow the optional PCI card retainer to be installed to secure the card (see Section 9.1).

- Detailed connector contact and housing designs are up to each connector vendor, as long as the requirements of form, fit, and function are met.
- Straddle mount connectors (connector that straddle the edge of a circuit board with one set of connections, such as the "A" side, connected to the top of the board and the other set of connections connected to the bottom of the board) are not explicitly covered in this specification

Formatted: Not Highlight

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Font color: Auto

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

but can be considered similar to surface mount connectors for many purposes such as high speed signaling considerations.

6.3. Signal Integrity Requirements and Test Procedures

6.3.1. Signal Integrity Requirements

The procedures outlined in the following ANSI Electronics Industry Alliance (EIA) standards documents shall be followed:

EIA 364-101 – Attenuation Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems

EIA 364-90 – Crosstalk Ratio Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems

EIA 364-108 – Impedance, Reflection Coefficient, Return Loss, and VSWR Measured in the Time and Frequency Domain Test Procedure for Electrical Connectors, Sockets, Cable Assemblies or Interconnection Systems

6.3.2. Signal Integrity Requirements and Test Procedures for 2.5 GT/s Support

A common electrical test fixture is specified and used for evaluating connector signal integrity. The test fixture will have 0.1524 mm (6.0 mil) wide 50 Ω single ended traces that must be uncoupled. The impedance variation of those traces shall be controlled within ±5%. Refer to the *PCI Express Connector High Speed Electrical Test Procedure* for detailed discussions on the test fixture.

Detailed testing procedures are specified in the *PCI Express Connector High Speed Electrical Test Procedure*. This document should be used in conjunction with the standard test fixture.

For the insertion loss and return loss tests, the measurement shall include 1.2-inch long PCB traces (0.6 inches on the system board and 0.6 inches on the add-in card). ~~Note that t~~The ~~edge fingeredge-finger~~ pad is not counted as ~~the~~ add-in card PCB trace~~. It~~, it is considered ~~to be~~ part of the connector interface. The 1.2-inch PCB trace included in the connector measurement is a part of the trace length allowed on the system board. See Section 4.7 for a discussion of the electrical budget.

Formatted: Not Highlight

Formatted: Not Highlight

Either single ended measurements that are processed to extract the differential characteristics or true differential measurements are allowed. The detailed definition and description of the test fixture and the measurement procedures are provided separately in a document entitled *PCI Express Connector High Speed Electrical Test Procedure*.

An additional consideration for the connector electrical performance is the connector-to-system board and the connector-to-add-in-card launches. The connector through hole pad and anti-pad sizes shall follow good electrical design practices to minimize impedance discontinuity. On the add-in card, the ground and power planes underneath the PCI Express high-speed signals (~~edge fingeredge-fingers~~) shall be removed. Otherwise, the ~~edge fingeredge-fingers~~ will have too much capacitance and greatly degrade connector performance. A more detailed discussion on the add-in card electrical design can be found in the *PCI Express Connector High Speed Electrical Test Procedure*.

Table 6-2~~Table 6-2~~~~Table 6-2~~ lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-2~~6-2~~: Signal Integrity Requirements and Test Procedures for 2.5 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in the *PCI Express Connector High Speed Electrical Test Procedure* document (see Note 1 below). 2. A common test fixture for connector characterization shall be used. 3. This is a differential insertion loss requirement. Either true differential measurements must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in the *PCI Express Connector High Speed Electrical Test Procedure* document (Note 1).	≤ 1 dB up to 1.25 GHz; ≤ [1.6*(F-1.25)+1] dB for 1.25 GHz < f ≤ 3.75 GHz (for example, ≤5 dB at f = 3.75 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard must be used with the following considerations: 1. The step-by-step measurement procedure is outlined in the *PCI Express Connector High Speed Electrical Test Procedure* document (Note 1). 2. A common test fixture for connector characterization shall be used. 3. This is a differential return loss requirement. Either true differential measurements must be made or post processing of the single ended measurements must be done to extract the differential characteristics of the connector. The methodology of doing so is covered in the *PCI Express Connector High Speed Electrical Test Procedure* document (Note 1).	≤ -12 dB up to 1.3 GHz; ≤ -7 dB for 1.3 GHz < f ≤ 2 GHz; ≤ -4 dB for 2 GHz < f ≤ 3.75 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max

Parameter	Procedure	Requirements
Differential Near End Crosstalk: DDNEXT	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 6-6~~Figure 6-6~~~~Figure 6-4~~. This is reflected in the measurement procedure. 2. The step-by-step measurement procedure is outlined in the *PCI Express Connector High Speed Electrical Test Procedure* document. 3. A common test fixture for connector characterization shall be used. 4. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. Either true differential measurements must be made or post processing of the single ended measurements must be done to extract the differential crosstalk of the connector. The methodology of doing so is covered in the *PCI Express Connector High Speed Electrical Test Procedure* document (see Note 1 below).	≤ -32 dB up to 1.25 GHz; ≤ -[32-2.4*(F-1.25)] dB for 1.25 GHz < f ≤ 3.75 GHz (for example, ≤ -26 dB at f = 3.75 GHz)
Jitter	By design; measurement not required.	10 ps max

Notes:
1. The *PCI Express Connector High Speed Electrical Test Procedure* is available separately.
2. A typical approach to making these measurements is with a network analyzer or a TDR oscilloscope. Differential measurements require the use of a two port (or a four port) instrument to measure the connector. The differential parameters may be measured directly if the equipment supports "True" differential excitation ("True" differential excitation is the simultaneous application of a signal to one line of the pair and a 180 degree phase shifted version of the signal to the second line of the pair). If single ended measurements are made, the differential connector parameters must be derived from the single ended measurements as defined in *the PCI Express Connector High Speed Electrical Test Procedure*.
3. The connector shall be targeted for a 100 Ω differential impedance.

Formatted: Font: Italic

In Figure 6-6~~Figure 6-6~~~~Figure 6-4~~, pairs marked as 11-9, 5-7, 15-13, and 17-19 are the adjacent pairs with respect to the victim pair 1-3.

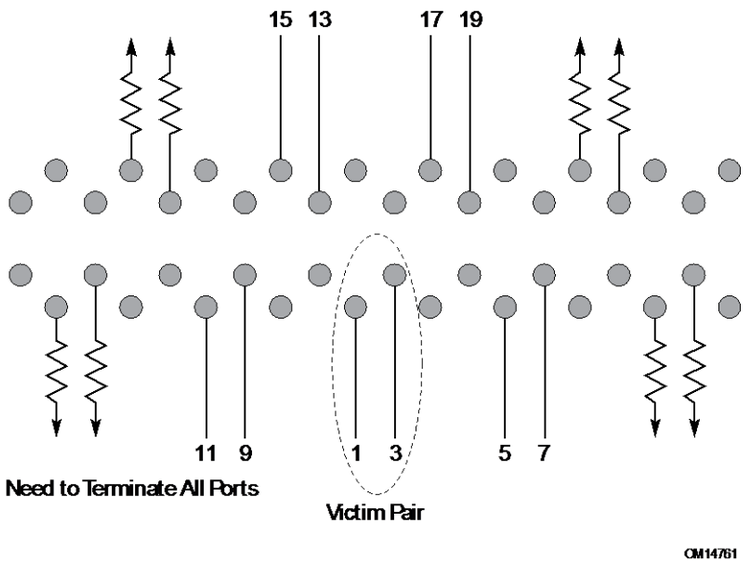


Figure 6-~~66-6~~: Illustration of Adjacent Pairs

6.3.3. Signal Integrity Requirements and Test Procedures for 5.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are deembeded from measurements. A section is provided with test fixture requirements and recommendations.

Table 6-3~~Table 6-3~~~~Table 6-3~~ lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-~~36-3~~: Signal Integrity Requirements and Test Procedures for 5.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.3.15~~.4.2~~. 3. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥ -2.5 dB at f = 5 GHz); ≥ -[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 7.5 GHz (for example, ≥-10 dB at f = 7.5 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.3.15~~.4.2~~. 3. The test fixture effect shall be removed. Refer to Note 1.	≤ -15 dB up to 3.0 GHz; ≤ -5 dB for 3.0 GHz < f ≤ 5 GHz; ≤ -1 dB for 5.0 GHz < f ≤ 7.5 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 6-6~~Figure 6-6~~~~Figure 6-4~~. 2. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz; ≤ -20 dB for 5.0 GHz < f ≤ 7.5 GHz

Notes:
1. The specified S parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

Formatted: Highlight

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

6.3.3.1 Test Fixture Requirements

The test fixture for connector S-parameter measurement should be designed and built to the following requirements:

The test fixture shall be an FR4-based PCB of the microstrip structure; the dielectric thickness or stackup shall be approximately 0.102 mm (4 mils).

The total thickness of the test fixture PCB shall be 1.57 mm (~~0.0~~62~~")~~ mils) and the test add-in card should be a break-out card fabricated in the same PCB panel for the fixture.

The measurement signals shall be launched into the connector from the top of the test fixture, capturing the through-hole stub effect.

Traces between the connector and measurement ports (SMA or microprobe) should be uncoupled.

The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.72 mm (1800 mils). The trace lengths between the connector and measurement port on the test baseboard and add-in card shall be equal. ~~Note that t~~The ~~edge finger~~edge-finger pad is not counted as ~~the~~ add-in card PCB trace; it is considered ~~as a~~ part of the connector interface.

All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ω with a tolerance of ±7%.

The test add-in card ~~edge finger~~edge-finger pads shall be fabricated per mechanical specification defined in Figure 6-5~~Figure 6-5Figure 6-3~~. The ground plane immediately underneath the ~~edge finger~~edge-finger pads must be removed.

The through-hole on the test board shall have the following stackup: 0.711 mm (28- mils) finished hole, 1.067 mm (42- mils) pad, and 1.473 mm (58- mil) anti-pad.

Use of SMA connectors is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a 60 ps rise time is recommended to be within 50 ±7 Ω.

If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

Formatted: Not Highlight

Formatted: Font color: Auto

Formatted: Font color: Auto

6.3.4. Signal Integrity Requirements and Test Procedures for 8.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are deembeded from measurements. A section is provided with test fixture requirements and recommendations.

Table 6-4~~Table 6-4~~~~Table 6-4~~ lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-~~4~~6-4: Signal Integrity Requirements and Test Procedures for 8.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.4.1. 3. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥ -0.5 dB up to 2.5 GHz; ≥ -[0.8*(f-2.5)+0.5] dB for 2.5 GHz < f ≤ 5 GHz (for example, ≥ -2.5 dB at f = 5 GHz); ≥ -[3.0*(f-5)+2.5] dB for 5 GHz < f ≤ 12 GHz (for example, ≥ -10 dB at f = 7.5 GHz)
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.4.1. 3. The test fixture effect shall be removed. Refer to Note 1.	≤ -15 dB up to 3.0 GHz; ≤ 5*f - 30 dB for 3.0 GHz < f ≤ 5 GHz; ≤ -1 dB for 5.0 GHz < f ≤ 12 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 6-~~6~~Figure 6-~~6~~Figure 6-4. 2. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	≤ -32 dB up to 2.5 GHz; ≤ -26 dB for 2.5 GHz < f ≤ 5.0 GHz; ≤ -20 dB for 5.0 GHz < f ≤ 10 GHz < -10 dB for 10 GHz < f ≤ 12 GHz

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

Notes:
1. The specified S-parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

6.3.4.1 Test Fixture Requirements

The test fixture for connector S-parameter measurement should be designed and built to the following requirements:

The test fixture shall be an FR4-based PCB of the microstrip structure; the dielectric thickness or stackup shall be approximately 0.~~102~~ 102 mm (~~4~~ 4 mils).

The total thickness of the test fixture PCB shall be 1.~~57~~ 57 mm (0.062") and the test add-in card should be a break-out card fabricated in the same PCB panel for the fixture.

The measurement signals shall be launched into the connector from the top of the test fixture, capturing the through-hole stub effect.

Traces between the connector and measurement ports (SMA or microprobe) should be uncoupled.

The trace lengths between the connector and measurement port shall be minimized. The maximum trace length shall not exceed 45.~~72~~ 72 mm (~~1800~~ 1800 mils). The trace lengths between the connector and measurement port on the test baseboard and add-in card shall be equal. ~~Note that t~~The ~~edge fingeredge-finger~~ pad is not counted as ~~the~~ add-in card PCB trace; it is considered ~~as a~~ part of the connector interface.

All of the traces on the test board and add-in card must be held to a characteristic impedance of 50 Ω with a tolerance of ±7%.

The test add-in card ~~edge fingeredge-finger~~ pads shall be fabricated per mechanical specification defined in ~~Figure 6-5Figure 6-5Figure 6-3~~. The ground plane immediately underneath the ~~edge fingeredge-finger~~ pads must be removed.

The through-hole on the test board shall have the following stackup: 0.~~711~~ 711 mm (28~~-~~ mils) finished hole, 1.~~067~~ 067 mm (42~~-~~ mils) pad, and 1.473~~-~~ mm (58~~-~~ mils) anti-pad.

Use of SMA connectors is recommended. The SMA launch structure shall be designed to minimize the connection discontinuity from SMA to the trace. The impedance range of the SMA seen from a TDR with a ~~30~~ 30 ps rise time is recommended to be within 50 ±~~7~~ 7 Ω.

If a fixture with other characteristics is used, the fixture effects must be reliably removed and must not impact measurement accuracy.

Formatted: Not Highlight

Formatted: Font color: Auto

Formatted: Font color: Auto

6.3.5. Signal Integrity Requirements and Test Procedures for 16.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects, not including the connector via, are deembeded from measurements. A section is provided with test fixture requirements and recommendations.

Table 6-4~~Table 6-4~~~~Table 6-4~~ lists the electrical signal integrity parameters, requirements, and test procedures.

~~TBD: Need to support both through hole and SMT.~~

Table 6-5: Signal Integrity Requirements and Test Procedures for 16.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 4. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 5. The test fixture shall meet the test fixture requirement defined in Section 6.3.4.1~~6.3.5.1~~. 6. The test fixture effect shall be removed from the measured S parameters. Refer to Note 1.	≥ -1 dB up to 8 GHz;
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 4. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 5. The test fixture shall meet the test fixture requirement in Section 6.3.4.1~~6.3.5.1~~. 6. The test fixture effect shall be removed. Refer to Note 1.	≤ -10 dB up to 8.0 GHz;
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 3. The crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as illustrated in Figure 6-6. 4. This is a differential crosstalk requirement between a victim differential signal pair and all of its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.	≤ -32 dB up to 8 GHz;

Notes:
1. The specified S-parameters requirements are for connector only, not including the test fixture effect. While the TRL calibration method is recommended, other calibration methods are allowed.

Formatted: Highlight

Formatted: Highlight

Formatted: Highlight

Formatted: Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 0" + Tab after: 0.25" + Indent at: 0.25"

6.3.5.1 Test Fixture Requirements

The test fixture for connector S-parameter measurement should be designed and built to the following requirements:

Test fixture requirements for both through-hole and SMT will be added in Rev 0.7

6.4. Connector Environmental and Other Requirements

6.4.1. Environmental Requirements

Connector environmental tests shall follow EIA-364-1000.01, Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications. The test groups/sequences and durations shall be derived from the following requirements:

Durability (mating/unmating) rating of 50 cycles

Field temperature: 65 °C

Field life: seven years

Since the connector defined in Section 6.2 has far more than 0.~~127~~127 mm wipe length, Test Group 6 in EIA-364-1000.01 is not required. Test Group 7 in EIA-364-1000.01 is optional since the durability cycles is ≤ 50. The temperature life test duration and the mixed flowing gas test duration values are derived from EIA 364-1000.01 based on the field temperature, using simple linear interpolation. Table 6-6~~Table 6-5~~Table 6-5 lists these values.

Table 6-6~~5~~6-5: Test Durations

Test	Duration/Temperature
Temperature Life	168 hours at 105 °C
Temperature Life (preconditioning)	92 hours at 105 °C
Mixed Flowing Gas	10 days

The low level contact resistance (LLCR) is required to be 30 mΩ or less, initially. ~~Note that t~~The contact resistance measurement points shall include the solder tail and the contact-mating interface, as illustrated in Figure 6-7~~Figure 6-7~~Figure 6-5. The resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading, shall not exceed the value that is to be specified by each OEM to best suit their needs.

Formatted: Font: Not Italic

Formatted: Not Highlight

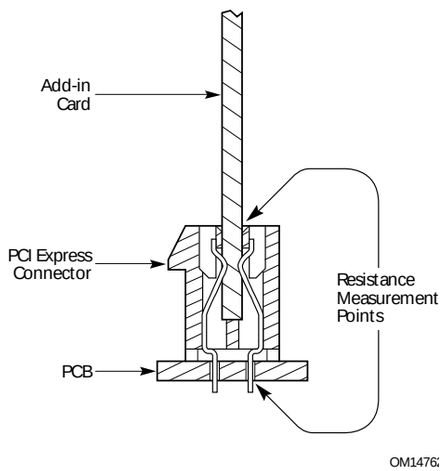


Figure 6-~~76~~ ~~7~~: Contact Resistance Measurement Points

To be sure that the environmental tests measure the stability of the connector, the add-in cards used shall have ~~edge-finger~~edge-finger tabs with a minimum plating thickness of 30 microinches of gold over 50 microinches of nickel *for the environmental test purpose only*. Furthermore, it is highly desirable that testing gives an indication of the stability of the connector when add-in cards at the lower and upper limit of the card thickness requirement are used. In any case, both the edge tab plating thickness and the card thickness shall be recorded in the environmental test report.

6.4.2. Mechanical Requirements

Table 6-7~~Table 6-6~~~~Table 6-6~~ lists the mechanical parameters and requirements. ~~Note that t~~The sample size shall follow Section 2.2.1 of EIA-364-1000.01.

Formatted: Not Highlight

Table 6-67~~6-6~~: Mechanical Test Procedures and Requirements

Test Description	Procedure	Requirement
Visual and dimensional inspections	EIA 364-18 Visual, dimensional, and functional per applicable quality inspection plan	Meets product drawing requirements
Insertion force	EIA 364-13 Measure the force necessary to mate the connector assemblies at a maximum rate of 12.5 mm (0.492 inches) per minute, using a steel gauge 1.~~70~~70 mm thick with a tolerance + 0.00, - .01 mm.	1.15 N maximum per contact pair
Removal force	EIA 364-13 Measure the force necessary to unmate the connector assemblies at maximum rate of 12.~~5~~5 mm (0.~~492~~492 inches) per minute, using a steel gauge 1.~~44~~44 mm thick with a tolerance + .01, - 0.~~00~~00 mm.	0.15 N minimum per contact pair

6.4.3. Current Rating Requirement

Table 6-8~~Table 6-7~~~~Table 6-7~~ lists the contact current rating requirement and test procedure.

Table 6-~~7~~8~~6-7~~: End of Life Current Rating Test Sequence

Test Order	Test	Procedure	Condition	Requirement
1	Contact current rating	EIA 364-70 method 2 The sample size is a minimum of three mated connectors. The sample shall be soldered on a PC board with the appropriate footprint. Wire the eight power pins (B1, B2, B3, A2, A3, B8, A9, and A10) and the eight nearest ground pins (A4, B4, B7, A12, B13, A15, B16, and B18) in a series circuit. The mated add-in card is included in this circuit. The add-in card shall have 1 oz. copper traces and its mating geometry shall conform to the applicable PCI Express drawings. A thermocouple of 30 AWG or less shall be placed on the card ~~edge finger~~edge-finger pad (pins B2 and A9) as close to the mating contact as possible. Conduct a temperature rise vs. current test.	Mated	1.1 A per pin minimum The temperature rise above ambient shall not exceed 30 °C. The ambient condition is still air at 25 °C.

6.4.4. Additional Considerations

Table 6-9~~Table 6-8~~~~Table 6-8~~ lists the additional requirements.

Table 6-~~8~~9~~6-8~~: Additional Requirements

Parameter	Procedure	Requirement
Flammability	UL94V-1 minimum	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.
Connector Color		Color of the connector should be black. Exceptions will be made for color coding schemes that call for a different color of this connector.

This specification does not attempt to define the connector requirements that are considered application-specific. It is up to the users and their connector suppliers to determine if additional requirements shall be added to satisfy the application needs. The system level shock and vibration tests are considered application-specific because results will depend on card weight and size, chassis stiffness, and retention mechanisms, as well as the connector. Therefore, those tests are not specified in the connector specification. It will be up to each system OEM to decide how the shock and vibration tests shall be done.

7

7. PCI Express 2 x 3 Auxiliary Power Connector Definition

This chapter defines the PCI Express 150 W add-in card power connector and cable assembly.

7.1. 6-Position Power Connector System Performance Requirements

The power connector system performance requirements are as follows:

Current Rating: 8.0 amperes per pin/position maximum to a 30 °C T-Rise above ambient temperature conditions at +12 VDC, all six contacts energized

Mated Connector Retention: 30.00 N minimum when plug pulled axially

7.2. 6-Position PCB Header

7.2.1. 6-Position R/A Thru-Hole PCB Header Assembly

Formatted: Tab stops: 0.88", List tab + Not at 1.5"

Figure 7-1~~Figure 7-1~~Figure 7-1 shows the details of a 6-position, R/A thru-hole PCB header assembly.

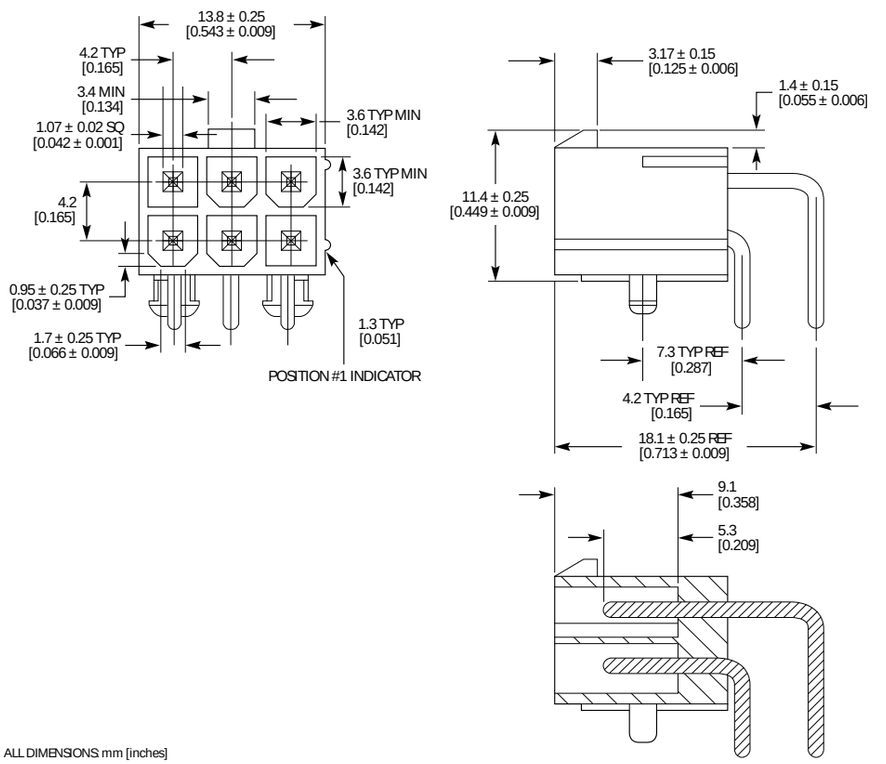


Figure 7-~~17 1~~: 6-Position R/A Thru-Hole PCB Header

R/A Thru-Hole PCB Header Assembly ~~Notes~~:

1. Housing Material: Thermoplastic, 94V-0 rated; Color: black
2. Pin Contact Base Material: Brass alloy or equivalent
3. Pin Contact Plating: Sn alloy
4. Connector Polarization: Per Figure 7-1~~Figure 7-1~~~~Figure 7-1~~

Formatted: Space After: 3 pt, Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 0" + Indent at: 0.25"

7.2.2. 6-Position R/A Thru-Hole Header Recommended PCB Footprint

Figure 7-2~~Figure 7-2~~Figure 7-2 shows the recommended PCB footprint for a 6-position, R/A thru-hole header.

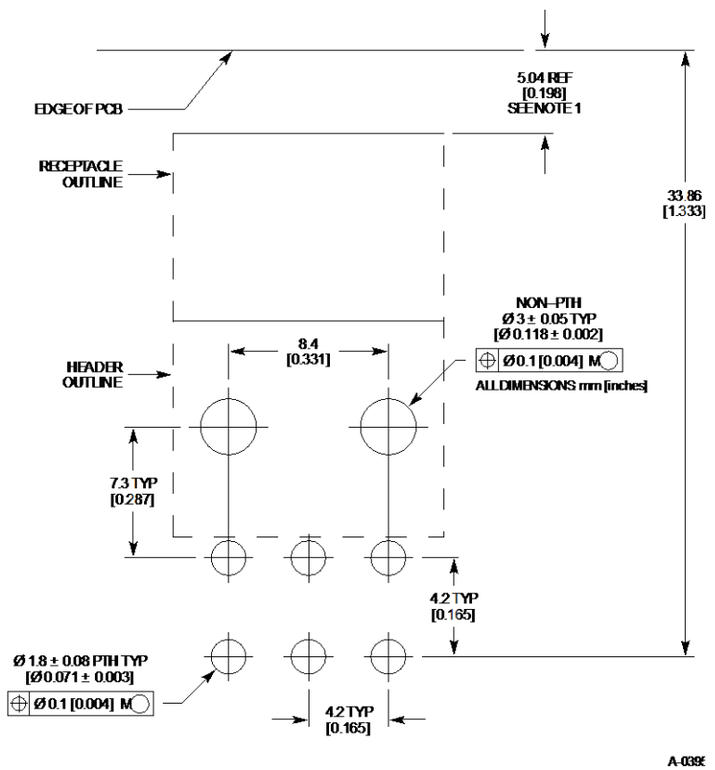


Figure 7-~~27~~2: 6-Position R/A Thru-Hole Header Recommended PCB Footprint

7.2.3. 6-Position R/A SMT PCB Header Assembly

Figure 7-3~~Figure 7-3~~~~Figure 7-3~~ shows the details of a 6-position, R/A SMT header assembly.

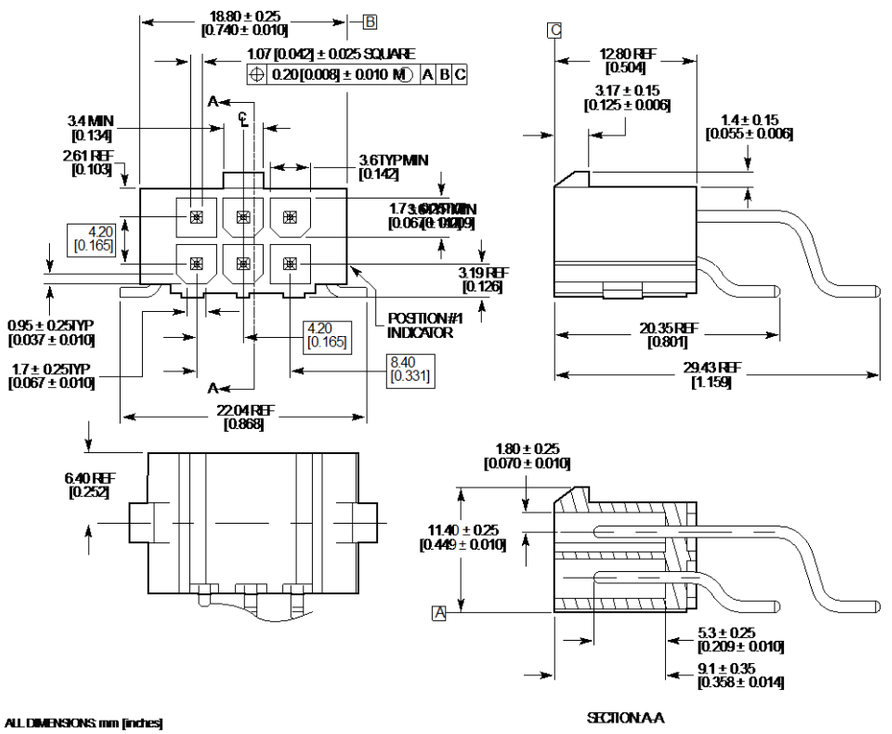


Figure 7-~~37~~ 3: R/A SMT PCB Header

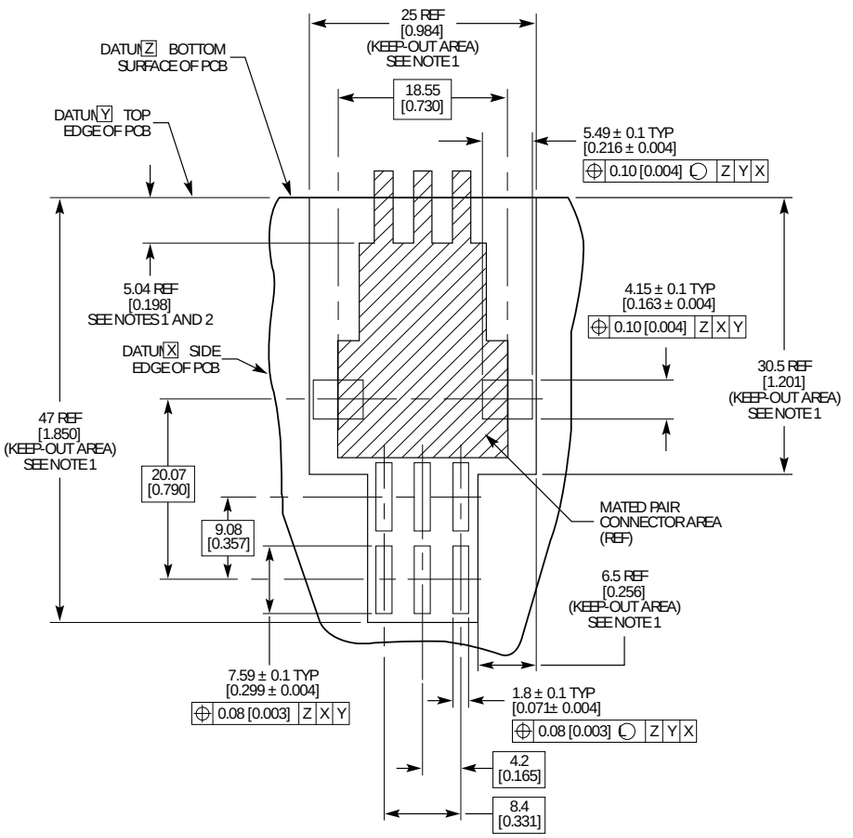
R/A SMT Header ~~Notes~~:

1. Housing Material: Thermoplastic, 94V-0 rated; Color: black
2. Pin Contact Base Material: Brass alloy or equivalent
3. Pin Contact Plating: Sn alloy
4. Connector Polarization: See Figure 7-3~~Figure 7-3~~~~Figure 7-3~~

Formatted: Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 0" + Indent at: 0.25"

7.2.4. R/A SMT Header Recommended PCB Footprint

Figure 7-4~~Figure 7-4~~~~Figure 7-4~~ shows the recommended PCB footprint for a 6-position, R/A SMT header.



NOTES:
1. KEEP-OUT DIMENSIONS SHOWN ARE BASED ON R/A HEADER PLACEMENT RELATIVE TO TOP EDGE OF PCB AND ARE FOR REFERENCE PURPOSES ONLY.
2. THIS RECOMMENDED PCB FOOTPRINT LOCATION ON THE GRAPHICS CARD IS BASED ON A SPECIFIC CONNECTOR PLACEMENT OF 5.04mm FORM THE TOP EDGE OF THE PCB TO THE BACK SURFACE OF THE MATING CABLE ASSEMBLY HOUSING AS SHOWN ABOVE AND IS FOR REFERENCE PURPOSES ONLY.
3. THIS RECOMMENDED PCB FOOTPRINT IS BASED ON THE R/A SMT HEADER CONFIGURATION SHOWN IN FIGURE 5. MODIFICATIONS TO THE R/A SMT HEADER REFERENCE DIMENSIONS (FIGURE 5) MAY REQUIRE A NEW PCB FOOTPRINT DESIGN.
4. ALL DIMENSIONS: mm [inches]

Figure 7-~~47-4~~: SMT Header Recommended PCB Footprint

150 W ~~ADD~~ IN CAR

Figure 7-~~4~~

A-0397

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: Auto, Line spacing: single

Formatted: Font: 8 pt, Small caps

Formatted: Small caps

Formatted: Font: 8 pt

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single

Formatted: Font: 8 pt

7.3. 6-Position Cable Assembly

Figure 7-5~~Figure 7-5~~Figure 7-5 shows the cable connector housing.

Cable Assembly Housing Details:

- Housing Material: Thermoplastic, 94V-0 rated; Color: black, special polarization per Figure 7-5~~Figure 7-5~~Figure 7-5
- Pin Contact Base Material: Brass alloy or equivalent
- Pin Contact Plating: Sn alloy

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

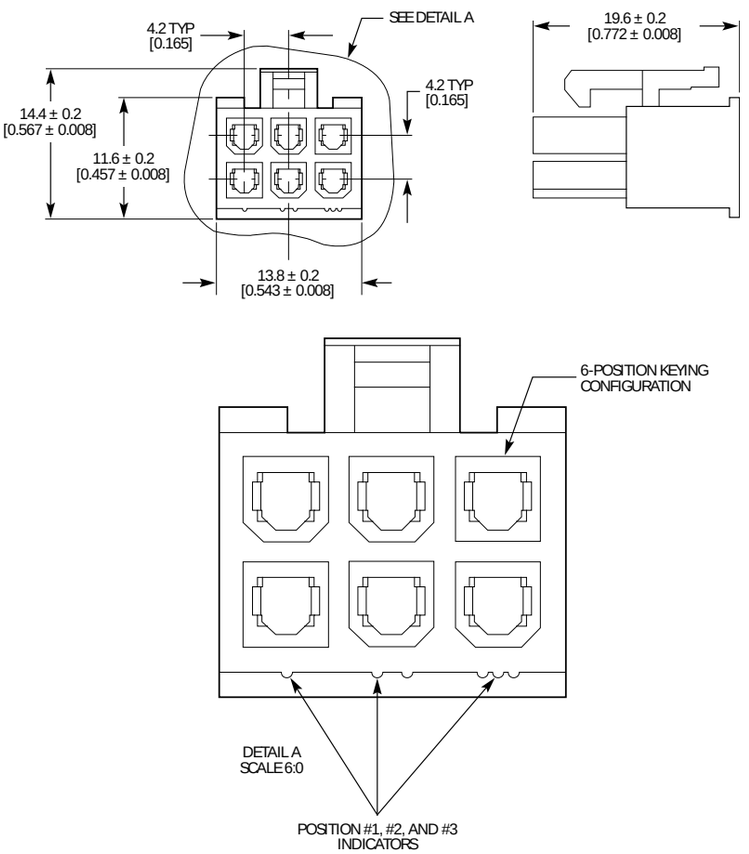


Figure 7-~~57-5~~: Cable Connector Housing

Cable Assembly Contact and Wire Details:

- Wire Size: 18 AWG
- Cable Bend Radius: 1xR minimum

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

7.4. Connector Mating-Unmating Keep-Out Area (Latch Lock Release)

The connector mating-unmating keep-out area is specified in Figure 7-6~~Figure 7-6~~~~Figure 7-6~~.

Formatted: Do not check spelling or grammar

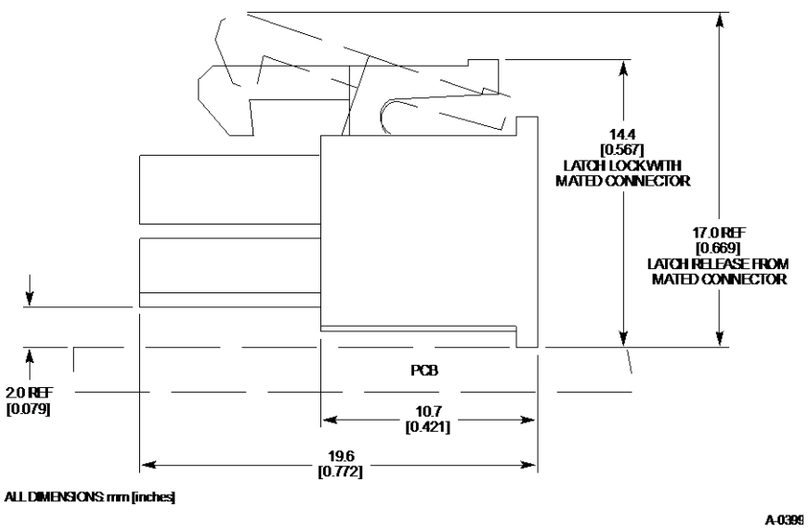


Figure 7-~~67-6~~: Connector Mating-Unmating Keep-Out Area (Latch Lock Release)

7.5. 6-Position Power Connector System Pin Assignment

Figure 7-7~~Figure 7-7~~Figure 7-7 and Table 7-1~~Table 7-1~~Table 7-1 show the pin-out for the PCI Express 150 W power connector.

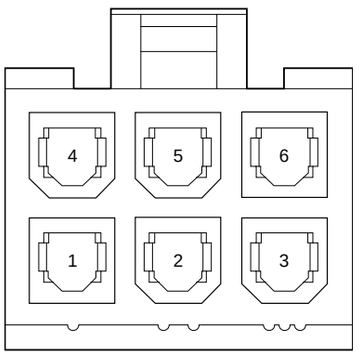


Figure 7-~~7-7~~7: 150 W Power Connector

Table 7-~~1~~7-1: 150 W Power Connector Pin-out

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Ground
5	Sense
6	Ground

IMPLEMENTATION NOTE

PCI Express 150 W Add-in Card Power Connector Sense Pin

The Sense pin on the PCI Express 150 W power connector must be connected to ground either directly in the power supply or via a jumper to an adjacent ground pin in the connector. This pin can be used by a PCI Express 150 W add-in card to detect if the PCI Express 150 W power connector is plugged.

Formatted: Font: Arial Black

Formatted: Font: Arial Black

Formatted: Font: 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt

Formatted: Space After: 3 pt

7.6. Additional Considerations

Table 7-2~~Table 7-2~~~~Table 7-2~~ lists the additional requirements for the PCI Express 150 W power connector.

Table 7-2~~7-2~~: PCI Express 150 W Power Connector Additional Requirements

Parameter	Procedure	Requirement
Flammability	UL94V-1 minimum	Material certification or certificate of compliance is required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.
Connector Color		The color of the connector should be black. Exceptions will be made for color coding schemes that call for a different color of this connector.

8

8. PCI Express 2 x 4 Auxiliary Power Connector Definition

This chapter defines the PCI Express 2 x 4 auxiliary power connector and cable assembly.

For backward compatibility, the 2 x 3 auxiliary power connector plug can be inserted into the 2 x 4 auxiliary power connector receptacle. The 2 x 4 receptacle is keyed such that the 2 x 3 connector plug needs to be properly aligned to plug in. Based on the sense codings in the 2 x 4 plug, a 225 W/300 W card with a 2 x 4 receptacle can detect if a 2 x 4 or a 2 x 3 plug is inserted. The 225 W/300 W card can then draw the appropriate power correspondingly.

The 2 x 4 auxiliary power connector plug should not be inserted into the 2 x 3 auxiliary power connector receptacle and is physically prevented from doing so. A dongle should be used for this purpose.

Figure 8-1~~Figure 8-1~~~~Figure 8-1~~ to Figure 8-3~~Figure 8-3~~~~Figure 8-3~~ depict the described auxiliary power connector mating scenarios.

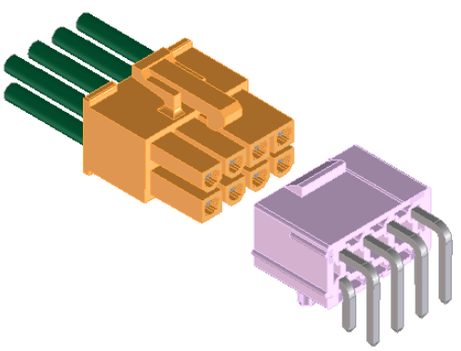


Figure 8-1~~8-1~~: 2 x 4 Plug Mating with a 2 x 4 Receptacle

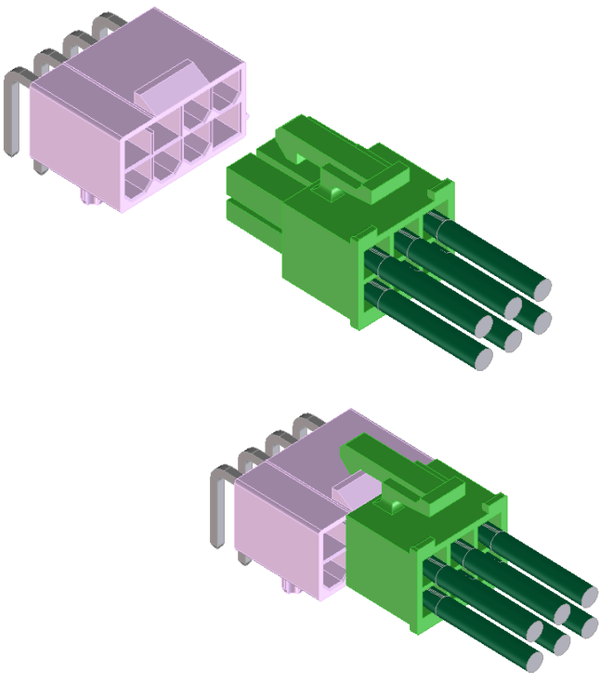


Figure 8-~~28-2~~: 2 x 3 Plug Mating with a 2 x 4 Receptacle

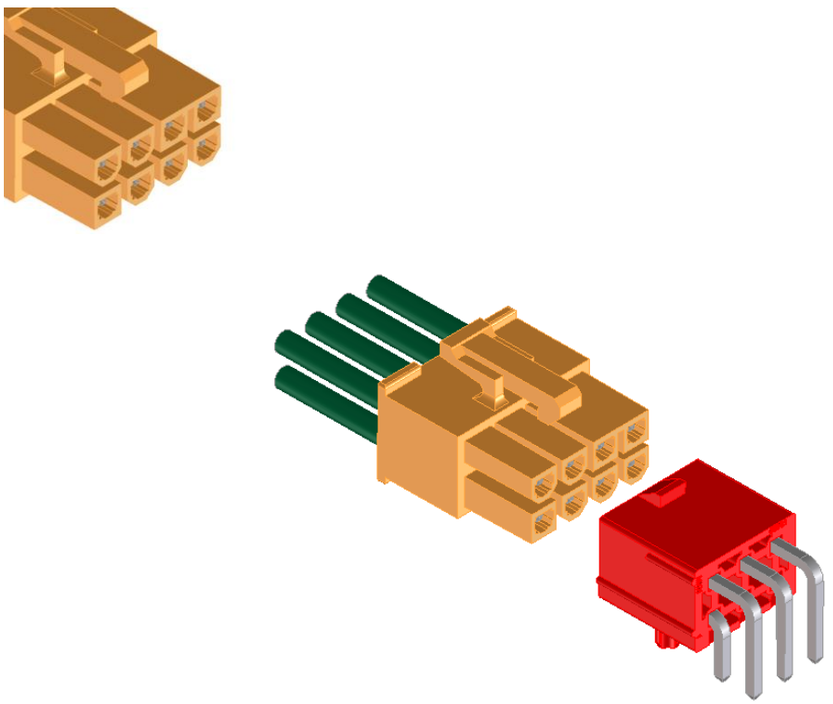


Figure 8-~~38-3~~: 2 x 4 Plug is Physically Prevented From Mating with a 2 x 3 Receptacle

8.1. 2 x 4 Auxiliary Power Connector Performance Requirements

The auxiliary power connector performance requirements are as follows:

Current Rating: 7.0 A per pin/position maximum to a 30 °C T-Rise above ambient temperature conditions at +12 VDC with all eight contacts energized

Mated Connector Retention: 30.00 N minimum when plug pulled axially

IMPLEMENTATION NOTE

Auxiliary Power Connector Current Rating

System integrators should ensure that the contacts used in auxiliary power connector are of the correct rating to meet the 7.0 A requirement. Appropriate derating practices should be used.

8.2. 2 x 4 Receptacle

8.2.1. Connector Drawing

Figure 8-4~~Figure 8-4~~~~Figure 8-4~~ shows the details of a 2 x 4 (eight-position), right-angle (R/A) through-hole connector.

~~Notes~~2 x 4 Receptacle:

1. Housing Material: Thermoplastic
2. Pin Contact Base Material: Brass Alloy or equivalent
3. Pin Contact Plating: Sn Alloy
4. An alignment rib is defined (detail A) to help guide the mating with a 2 x 3 plug.
5. Though not defined in this specification, a vertical receptacle, in which the mating cable plug is perpendicular to the add-in card, is also allowed. Add-in card manufacturers can work with their connector vendors to enable such a connector.
6. All dimensions are in mm [inches].

Formatted: Font: Arial Black

Formatted: Font: Arial Black

Formatted: Left

Formatted: Font: 11 pt, Bold

Formatted: Left, Space Before: 3 pt, After: 0 pt

Formatted: Space After: 3 pt

Formatted: Not Highlight

Formatted: Highlight

Formatted: Indent: Left: 0", Hanging: 0.38", Numbered + Level: 1 + Numbering Style: 1, 2, 3, … + Start at: 1 + Alignment: Left + Aligned at: 0" + Indent at: 0.25"

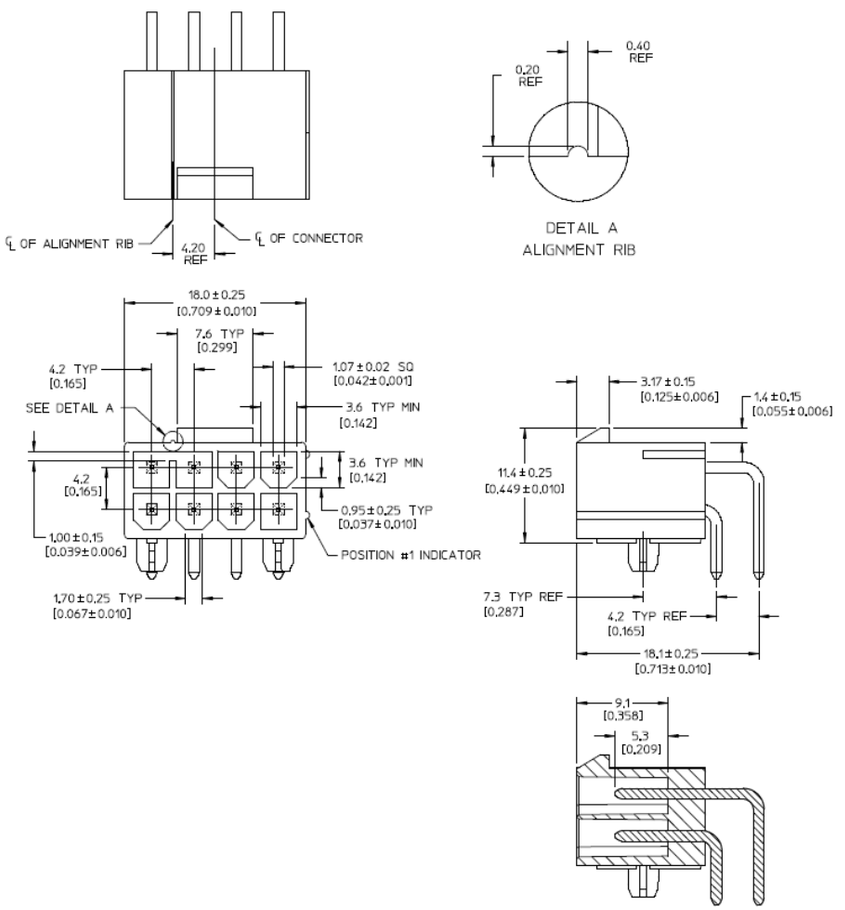


Figure 8-~~48~~-4: 2 x 4 R/A Through-Hole Receptacle Drawing

8.2.2. PCB Footprint

Figure 8-5~~Figure 8-5~~~~Figure 8-5~~ shows the recommended PCB footprint for the 2 x 4 R/A receptacle.

~~Note:~~ All dimensions are in mm [inches].

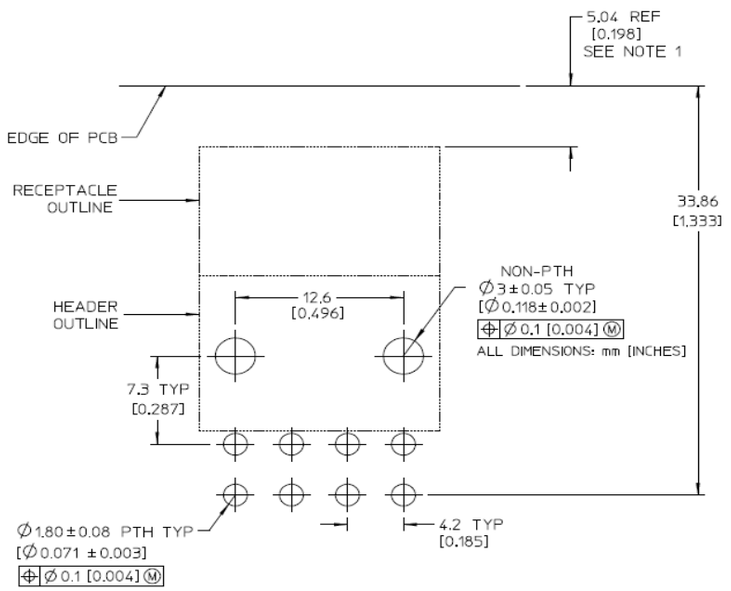


Figure 8-~~58 5~~: 2 x 4 R/A Through-Hole Recptacle Recommended PCB Footprint

8.3. Cable Assembly

Figure 8-6~~Figure 8-6~~Figure 8-6 shows the cable plug connector housing.

~~Note:~~ All dimensions are in mm [inches].

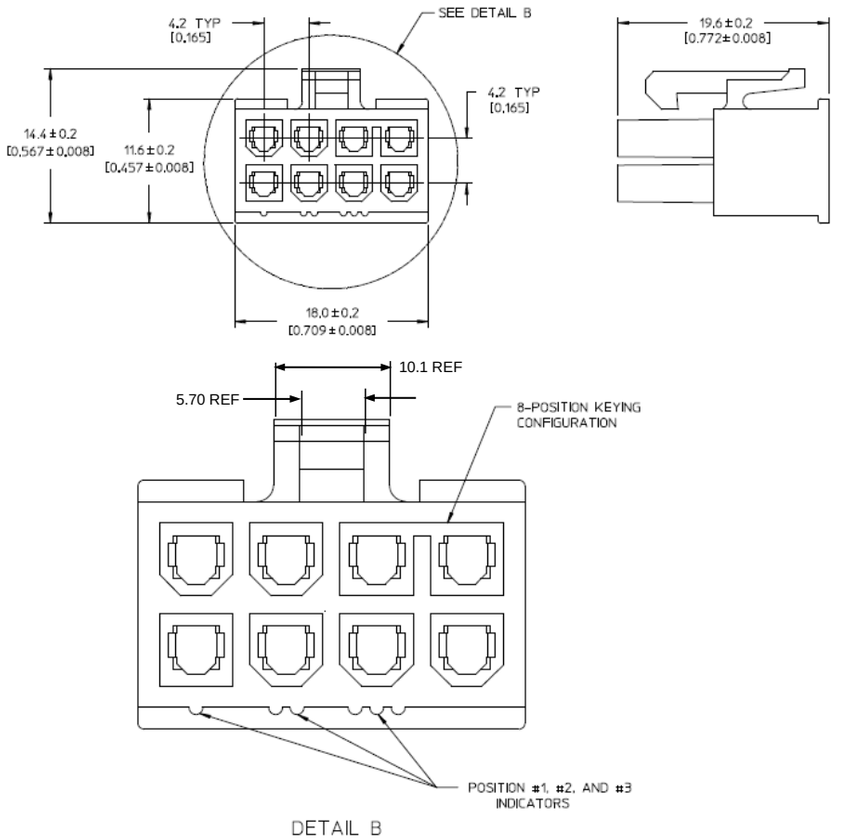


Figure 8-~~6~~8 ~~6~~: Cable Plug Connector Housing

Formatted: Indent: Left: 0", Space After: Auto, Line spacing: single

Formatted: Indent: Left: 0", Space After: Auto, Line spacing: single

Cable Assembly Contact and Housing Details:

Housing Material: Thermoplastic; special polarization per Figure 8-6~~Figure 8-6~~~~Figure 8-6~~

Pin Contact Base Material: Brass alloy or equivalent

Pin Contact Plating: Sn alloy

Wire Details:

Wire Size: 18 AWG

Cable Bend Radius: 1xR minimum

~~-~~IMPLEMENTATION NOTE

Modular Plug Connector Assembly

A 2 x 4 plug connector can be designed with a 2 x 3 plug module and a 2 x 1 plug module to form a 2 x 4 modular plug connector such that it can be plugged into a 2 x 4 or 2 x 3 receptacle.Cable assembly vendors should design the Latch Lock Hook and Release Handle with the dimensions ~~noted~~ defined in Figure 8-7~~Figure 8-7~~~~Figure 8-7~~ to ensure that the connector locks securely when plugged into a 2 x 4 or a 2 x 3 receptacle. The rest of the dimensions are the same as shown in Figure 8-6~~Figure 8-6~~~~Figure 8-6~~.

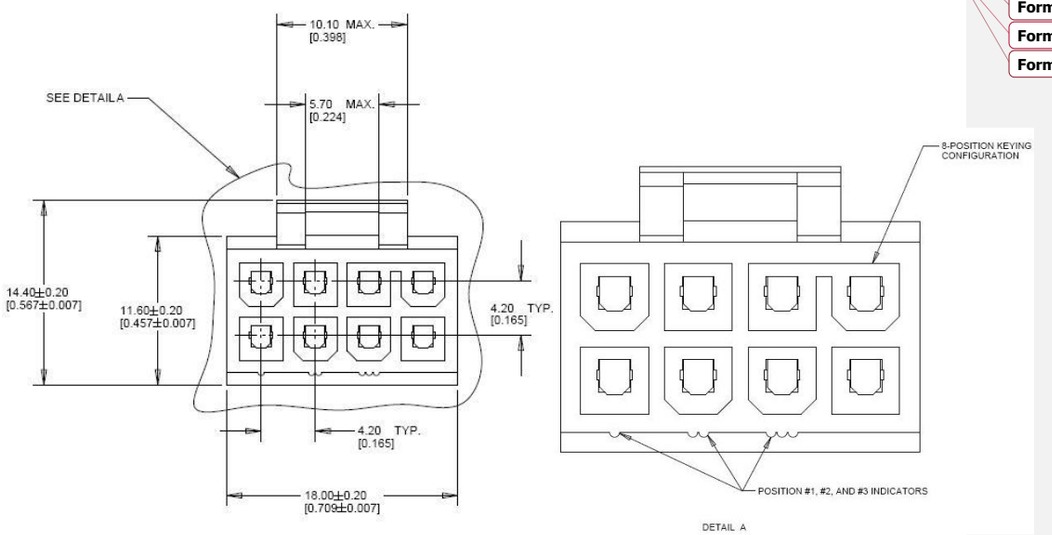


Figure 8-~~7~~8 ~~7~~: Modular Plug Connector Housing (All Dimensions in mm [Inches])

Formatted: Font: Arial Black
Formatted: Left
Formatted: Font: Arial Black
Formatted: Font: 11 pt, Bold
Formatted: Left, Space Before: 3 pt, After: 0 pt
Formatted: Space After: 3 pt
Formatted: Font: (Default) Arial, 10 pt
Formatted: Font: (Default) Arial, 10 pt
Formatted: Font: (Default) Arial, 10 pt
Formatted: Font: (Default) Arial, 10 pt
Formatted: FigureTitle

8.4. Connector Mating-Unmating Keep-Out Area (Latch Lock Release)

The connector mating-unmating keep-out area is specified in Figure 8-8~~Figure 8-8~~~~Figure 8-8~~.

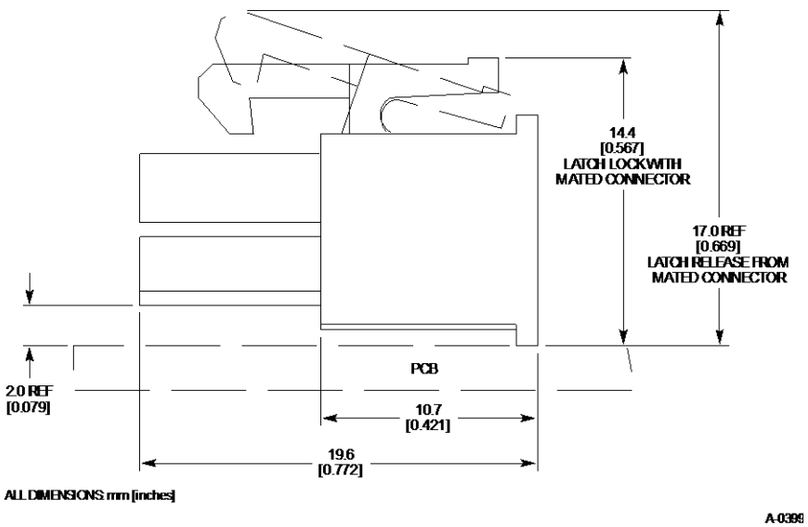


Figure 8-~~8-8~~: Connector Mating-Unmating Keep-Out Area (Latch Lock Release)

8.5. 2 x 4 Auxiliary Power Connector System Pin Assignment

Figure 8-9~~Figure 8-9~~Figure 8-9 and Figure 8-10~~Figure 8-10~~Figure 8-10 show the pin-out for the 2 x 4 auxiliary power connector.

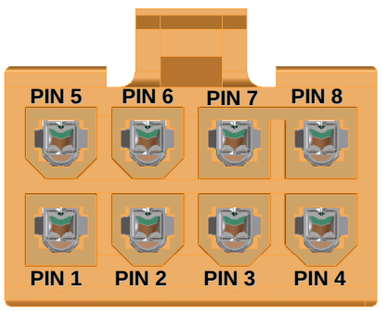


Figure 8-~~9~~8-9: 2 x 4 Auxiliary Power Connector Plug Side Pin-out

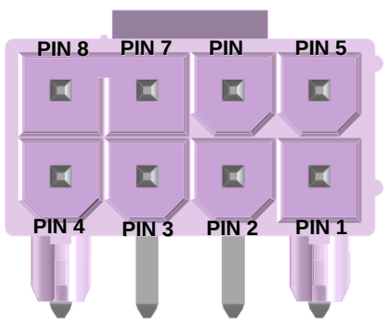


Figure 8-~~10~~8-10: 2 x 4 Auxiliary Power Connector Receptacle Side Pin-out

Table 8-1~~Table 8-1~~Table 8-1 and Table 8-2~~Table 8-2~~Table 8-2 show the 2 x 4 pin-out assignments. A ~~225~~ 225 W/~~300~~ 300 W card with a 2 x 4 auxiliary power connector receptacle, decodes the sense coding to determine how much power to draw from the 2 x 4 auxiliary power connector.

Table 8-~~18 1~~: 2 x 4 Auxiliary Power Connector Pin-out Assignment

Pin	Signal
1	+12 V
2	+12 V
3	+12 V
4	Sense1
5	Ground
6	Sense0
7	Ground
8	Ground

Table 8-~~28 2~~: Sense Pins Decoding by a Graphics Card

Sense1	Sense0	Comment
Ground	Ground	A 2 x 4 auxiliary power connector is plugged into the card. The card can draw up to ~~150~~ 150 W from the auxiliary power connector.
Ground	Open	Reserved
Open	Ground	A 2 x 3 auxiliary power connector is plugged into the card. The graphics card can only draw up to ~~75~~ 75 W from the auxiliary power connector.
Open	Open	No auxiliary power connector is plugged in.

For a sense pin that needs to be grounded, it must be connected to ground either directly in the power supply or via a jumper to an adjacent ground pin in the connector. The sense pins are used by a PCI Express ~~225~~ 225 W/~~300~~ 300 W card to detect how much power to draw from the auxiliary power connector.

A 2 x 4 auxiliary power connector plug from the power supply unit must not use the ~~75~~ 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

For informational purposes, Figure 8-11~~Figure 8-11~~~~Figure 8-11~~ shows the 2 x 3 auxiliary power connector pin-out. Table 8-3~~Table 8-3~~~~Table 8-3~~ shows how the pins are mapped when a 2 x 3 plug is inserted into a 2 x 4 receptacle.

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

Formatted: Check spelling and grammar

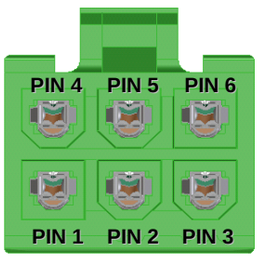


Figure 8-118 11: 2 x 3 Auxiliary Power Connector Pin-out

Table 8-38 3: 2 x 3 Plug to 2 x 4 Receptacle Pin Mapping

2 x 3 Plug	2 x 4 Receptacle	Signal
1	1	+12 V
2	2	+12 V
3	3	+12 V
NA	4	Sense1
4	5	Ground
5	6	Sense0
6	7	Ground
NA	8	Ground

8.6. Additional Considerations

Table 8-4Table 8-4Table 8-4 lists the additional requirements for the PCI Express 2 x 4 auxiliary power connector.

Table 8-48 4: Additional Requirements

Parameter	Procedure	Requirement
Flammability	UL94V-1 minimum	Material certification or certificate of compliance required with each lot to satisfy the Underwriters Laboratories follow-up service requirements.
Lead-free soldering		Connector must be compatible with lead free soldering process.
Connector Color		Color of the connector should be black. Exceptions will be made for color coding schemes that call for a different color of this connector.

9

9. Add-in Card Form Factors and Implementation

9.1. Add-in Card Form Factors

To enable the reuse of existing chassis slots, the PCI Express add-in cards are similar to the PCI add-in card form factor. Two PCI Express add-in card heights are defined: the standard height of 111.~~28~~28 mm (4.~~376~~376 inches) maximum and the low profile of 68.~~90~~90 mm (2.~~731~~731 inches) maximum. ~~Note that~~The card height is measured from the bottom of the ~~edge fingeredge-finger~~ to the top of the card (see Figure 9-1~~Figure 9-1Figure 9-1~~ and Figure 9-4~~Figure 9-4Figure 9-4~~). A PCI Express DUAL-SLOT add-in card has the same dimensions as a standard height full length card, except the component side height restriction is reduced to 34.80 mm. A TRIPLE-SLOT add-in card has the same dimensions as a standard height full length card, except the component side height restriction is 55.~~12~~12 mm. Table 9-1~~Table 9-1Table 9-1~~ lists the add-in card sizes.

Table 9-~~19-1~~: Add-in Card Sizes

Add-in Card	Height	Length[4]
Standard height	111.28 mm (4.381 inches) maximum	See Figure 9-2.
Low profile	68.90 mm (2.731 inches) maximum	See Figure 9-8.

~~It should be noted that t~~The maximum length specifies what the system design must accommodate. An add-in card can be any length up to the maximum for a particular length interval. For example, a standard height card with a 177.80 mm (7.00 inch) length can be installed in a system that accommodates 241.30 mm (9.5 inches) maximum length cards, but a system that only accommodates 167.65 mm (6.6 inches) maximum length cards will not support this card.

IMPLEMENTATION NOTE

PCI Express Card Length

Not all system designs will support 312 mm full length cards. It is strongly recommended that PCI Express add-in cards be designed with a 241.30 mm (9.5 inches) maximum length. This applies to SINGLE-SLOT, DUAL-SLOT and TRIPPLE-SLOT add-in card designs.

[4] Not all system designs will support this length of add-in card. It is strongly recommended that standard height add-in cards be designed with a 241.30 mm (9.~~5~~5 inches) maximum length.

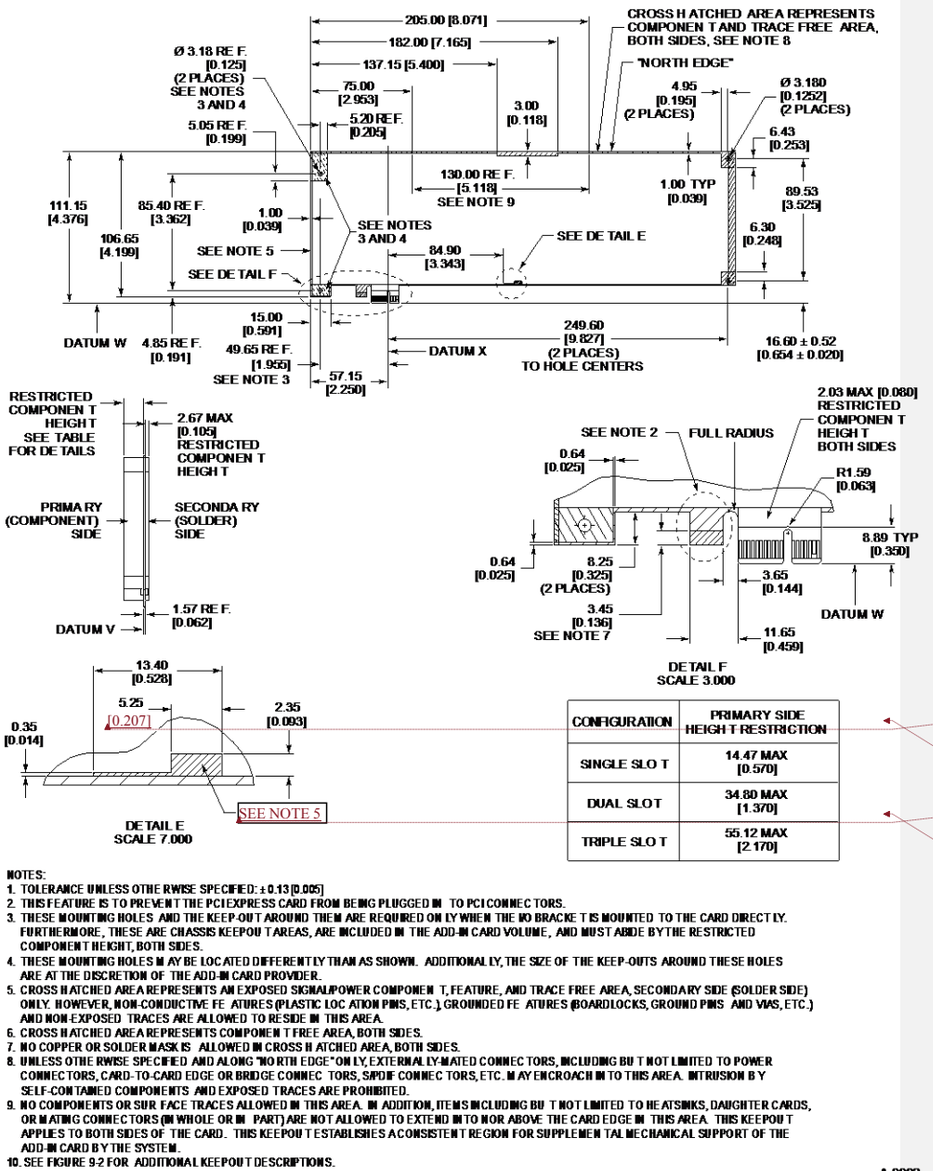
Formatted: Not Highlight
Field Code Changed
Field Code Changed
Formatted: Font: Arial Black
Formatted: Font: Bold
Formatted: Space Before: 3 pt, After: 0 pt

Figure 9-1~~Figure 9-1~~Figure 9-1 and Figure 9-3~~Figure 9-3~~Figure 9-3 show the standard PCI Express card form factor without and with the I/O bracket, respectively.

All the figures need to be checked and updated to conform to latest agreed dimensions (including long gold finger ECN). Who will do this and can results be made available in SVG file format?

Formatted: Highlight

Formatted: Highlight



CONFIGURATION	PRIMARY SIDE HEIGHT RESTRICTION
SINGLE SLOT	14.47 MAX [0.570]
DUAL SLOT	34.80 MAX [1.370]
TRIPLE SLOT	55.12 MAX [2.170]

NOTES:
1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
2. THIS FEATURE IS TO PREVENT THE PCI EXPRESS CARD FROM BEING PLUGGED IN TO PCI CONNECTORS.
3. THESE MOUNTING HOLES AND THE KEEP-OUT AROUND THEM ARE REQUIRED ONLY WHEN THE IO BRACKET IS MOUNTED TO THE CARD DIRECTLY. FURTHERMORE, THESE ARE CHASSIS KEEPOUT AREAS, ARE INCLUDED IN THE ADD-IN CARD VOLUME, AND MUST ABIDE BY THE RESTRICTED COMPONENT HEIGHT, BOTH SIDES.
4. THESE MOUNTING HOLES MAY BE LOCATED DIFFERENTLY THAN AS SHOWN. ADDITIONALLY, THE SIZE OF THE KEEP-OUTS AROUND THESE HOLES ARE AT THE DISCRETION OF THE ADD-IN CARD PROVIDER.
5. CROSS HATCHED AREA REPRESENTS AN EXPOSED SIGNAL/POWER COMPONENT, FEATURE, AND TRACE FREE AREA, SECONDARY SIDE (SOLDER SIDE) ONLY. HOWEVER, NON-CONDUCTIVE FEATURES (PLASTIC LOCATION PINS, ETC.), GROUNDED FEATURES (BOARDLOCKS, GROUND PINS AND VIAS, ETC.) AND NON-EXPOSED TRACES ARE ALLOWED TO RESIDE IN THIS AREA.
6. CROSS HATCHED AREA REPRESENTS COMPONENT FREE AREA, BOTH SIDES.
7. NO COPPER OR SOLDER MASK IS ALLOWED IN CROSS HATCHED AREA, BOTH SIDES.
8. UNLESS OTHERWISE SPECIFIED AND ALONG "NORTH EDGE" ONLY, EXTERNALLY-MATED CONNECTORS, INCLUDING BUT NOT LIMITED TO POWER CONNECTORS, CARD-TO-CARD EDGE OR BRIDGE CONNECTORS, SPDIF CONNECTORS, ETC. MAY ENCROACH IN TO THIS AREA. INTRUSION BY SELF-CONTAINED COMPONENTS AND EXPOSED TRACES ARE PROHIBITED.
9. NO COMPONENTS OR SURFACE TRACES ALLOWED IN THIS AREA. IN ADDITION, ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND IN TO NOR ABOVE THE CARD EDGE IN THIS AREA. THIS KEEPOUT APPLIES TO BOTH SIDES OF THE CARD. THIS KEEPOUT ESTABLISHES A CONSISTENT REGION FOR SUPPLEMENTAL MECHANICAL SUPPORT OF THE ADD-IN CARD BY THE SYSTEM.
10. SEE FIGURE 9-2 FOR ADDITIONAL KEEPOUT DESCRIPTIONS.

A-0902

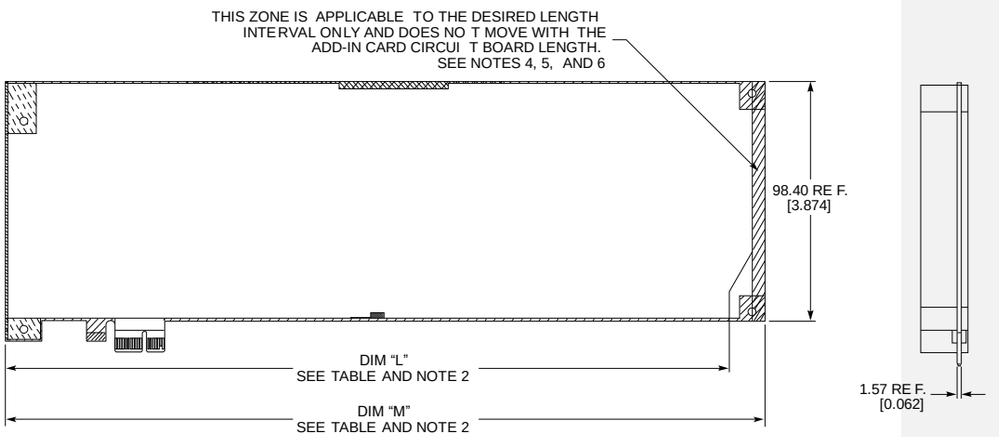
Figure 9-~~19-1~~: Standard Height PCI Express Add-in Card without the I/O Bracket

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single



LENGTH INTERVAL	DIM "L"	DIM "M"
HALF LENGTH	162.57 [6.400]	167.65 MAX [6.600]
THREE-QUARTER LENGTH	248.92 [9.800]	254.00 MAX [10.00]
FULL LENGTH	306.92 [12.083]	312.00 MAX [12.283]

NOTES:

1 TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]

2 DIMENSIONS ESTABLISH A CONSISTENT VOLUME FOR END CARD MECHANICAL SUPPORT.

3 FOR EACH LENGTH INTERVAL, DIMENSION "M" ALSO DESCRIBES THE MAXIMUM OVERALL LENGTH OF THE ADD-IN CARD ASSEMBLY.

4 FOR EACH DESIRED LENGTH INTERVAL, FEATURES OF THE ADD-IN CARD ASSEMBLY MUST INTERSECT WITH THIS VOLUME. IF PART OF THE ADD-IN CARD CIRCUIT BOARD, THIS MUST BE A COMPONENT AND SURFACE TRACE FREE AREA, BOTH SIDES.

5 FOR EACH DESIRED LENGTH INTERVAL, SYSTEMS MUST ACCOMODATE THE ENTIRE DESCRIBE VOLUME. OTHERWISE, ISSUES INCLUDING BUT NOT LIMITED TO NON-RETENTION OF ADD-IN CARD, FIT INTERFERENCE, ETC. COULD OCCUR.

6 FOR THE FULL LENGTH INTERVAL ONLY, ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO THIS AREA. THIS KEEPOUT APPLIES TO BOTH SIDES OF THE CARD. THESE ADDITIONAL COMPONENT AND TRACE RESTRICTIONS ARE DESIRED BUT NOT REQUIRED FOR THE HALF-LENGTH AND THREE QUARTER LENGTH INTERVALS.

A-0903

Figure 9-~~29-2~~: Chassis Interface Zones on Right/East Edge of Add-in Card

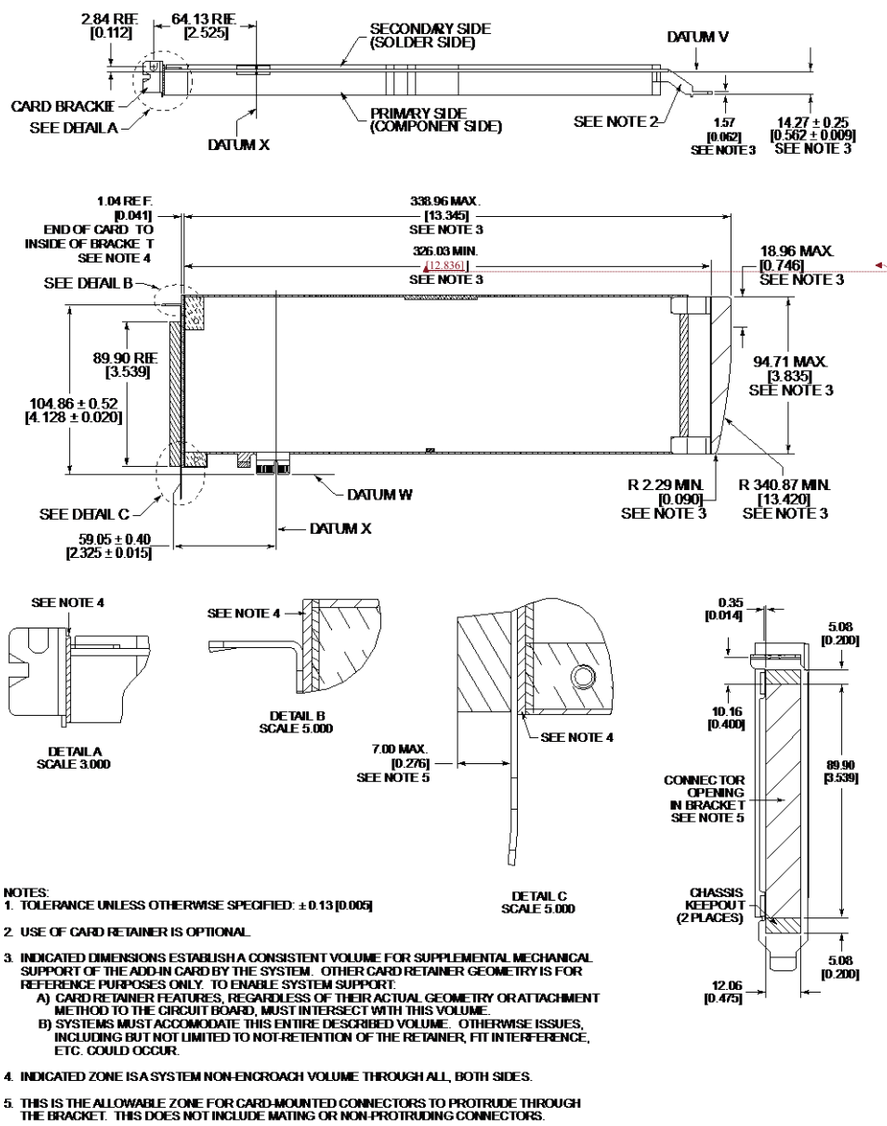


Figure 9-~~39-3~~: Standard Height PCI Express Add-in Card with the I/O Bracket and Card Retainer

Formatted: Font: 6 pt

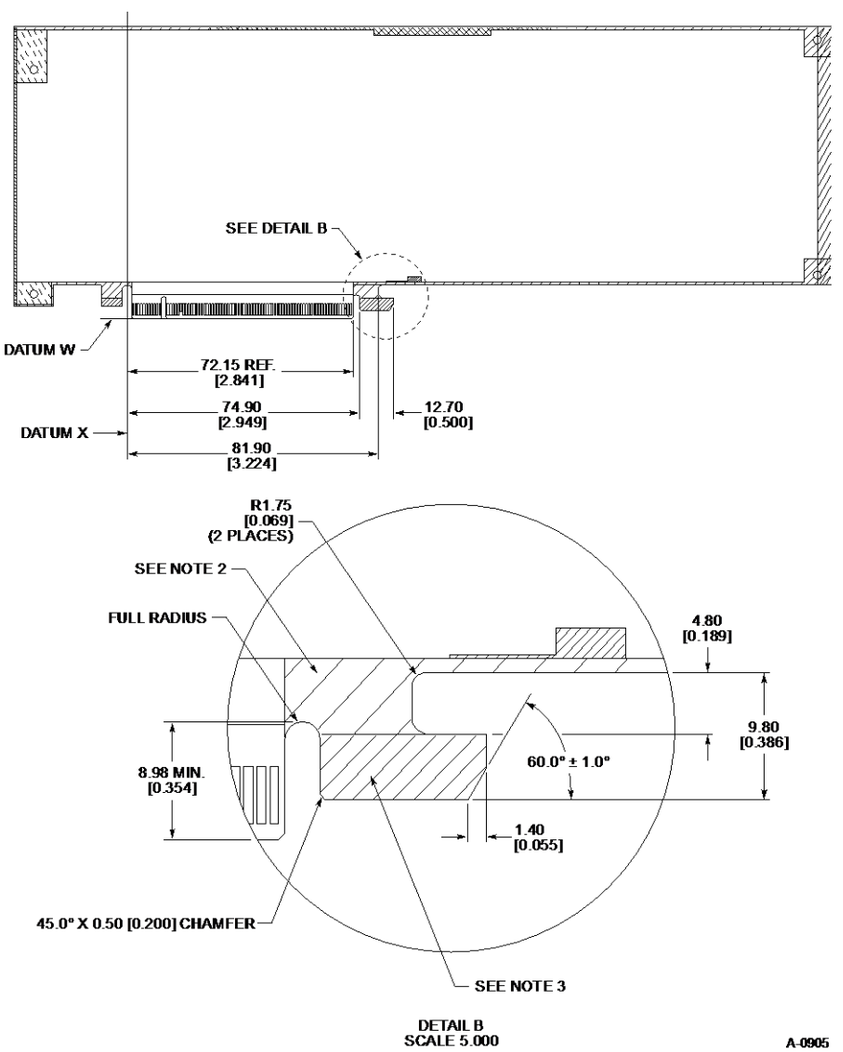
Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single

The mounting holes illustrated in Figure 9-1~~Figure 9-1~~~~Figure 9-1~~ are required only on the right end of the full-length card (312.00~~-~~ mm). Those holes may be needed to install an optional PCI add-in card retainer.

The mounting holes and keep-out zones around them marked as note 3 in Figure 9-1~~Figure 9-1~~~~Figure 9-1~~ may be used on those cards in which the I/O bracket is mounted to the card directly and are for reference purposes only. The purpose of this keep-out is to ensure that the card cannot short out on the I/O bracket. Add-in card providers should ensure that their card cannot short out the I/O bracket. On full-length cards, a keep-out of 5.08~~-~~mm is required to prevent card components from being damaged by the system's card guides (see Figure 9-1~~Figure 9-1~~~~Figure 9-1~~).

All graphics cards are required to be retention ready as defined in Section 9.2. This retention ready requirement may also apply to x1, x4, x8, or x16 I/O cards at each OEM, or add-in card manufacturer's discretion. See Section 9.2 for more information.

Special attention shall be given to high mass add-in cards. This specification defines the additional feature and keepouts for high-mass cards for card retention shown in Figure 9-4~~Figure 9-4~~~~Figure 9-4~~. This retention feature is not limited to higher-mass cards, and may be used by any card.



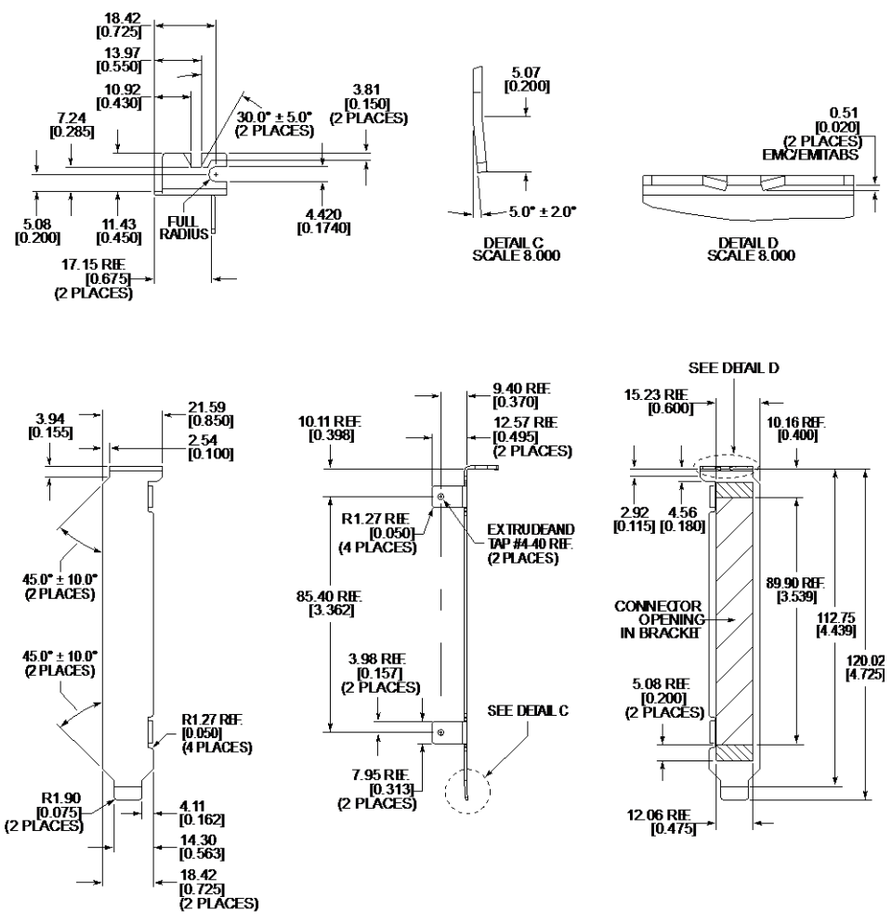
NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
2. CROSS HATCHED AREA REPRESENTS COMPONENT FREE AREA, BOTH SIDES.
3. NO COPPER OR SOLDER MASK IS ALLOWED IN CROSS HATCHED AREA, BOTH SIDES.

Figure 9-~~49~~ ~~4~~: Additional Feature and Keepouts for a High Mass Card

The 3.0 mm keepout on the top of the card is to accommodate system or chassis level card retention solutions at each OEM's discretion. To facilitate a chassis level retention solution, the height of the standard height graphics card is required to be fixed: 111.15 mm ±0.13 mm. The "hockey stick" shaped feature and keepout defined on the bottom of the card is to allow retention mechanisms either mounted directly on the system board or integrated into the connector. This feature and keepout are also required for the low profile graphics card.

All retention mechanisms that are intended for high mass cards must use the feature/keepout defined in Figure 9-4~~Figure 9-4~~~~Figure 9-4~~. But the specific retention mechanism design is system manufacturers' choice. Figure 9-5~~Figure 9-5~~~~Figure 9-5~~ shows the standard PCI Express I/O bracket, which is the same as the PCI bracket. The mounting tabs of the bracket shown in Figure 9-5~~Figure 9-5~~~~Figure 9-5~~ are to be mounted onto the secondary side of the card, as illustrated in Figure 9-3~~Figure 9-3~~~~Figure 9-3~~. However, a user also has the option to have a bracket with the mounting tabs mounted onto the primary side of the card. Exact locations of contact between the bracket and the add-in card PCB (and the associated keepout zones) are at the discretion of the add-in card provider and should not be assumed to be fixed by the system integrator for additional card retention. Any dimensions in figures which describe geometry for "PCB attach" are REFERENCE.



NOTES:
1. MATERIAL: 0.86 ± 0.08 [0.034 ± 0.003]THICK (20 GA)

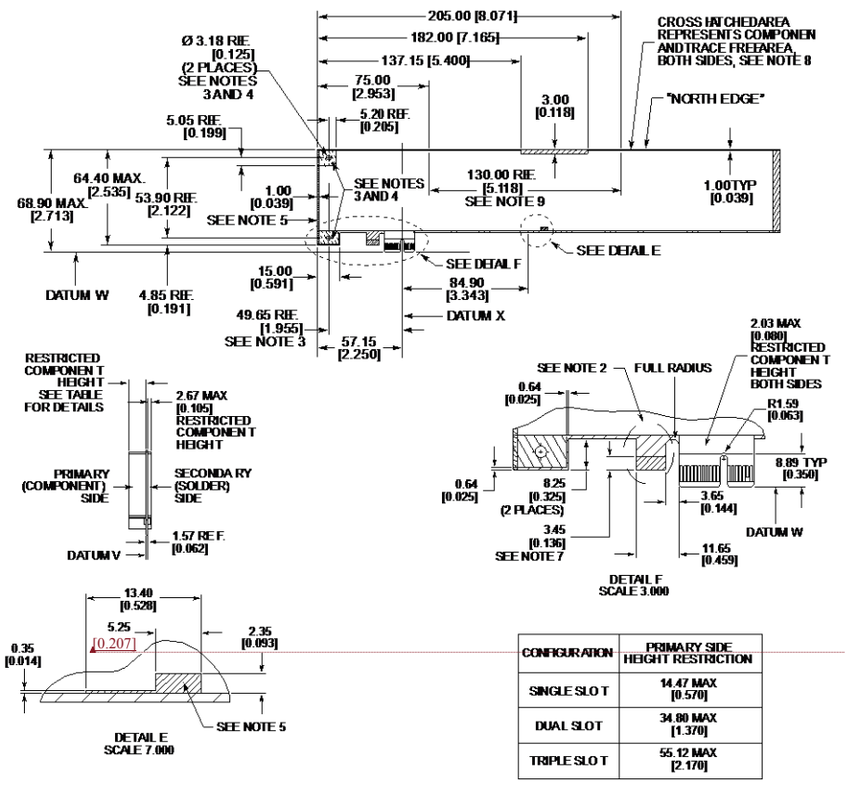
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25 [± 0.010]

A-0906

Figure 9-~~59-5~~: Standard Add-in Card I/O Bracket

The detailed add-in card ~~edge-finger~~edge-finger dimensions are defined in Section 6.2, which describes the connector mating interface. The edge-finger portions of the PCI Express cards are required to have bevels or chamfers as defined in Figure 6-5~~Figure 6-5~~~~Figure 6-3~~.

Figure 9-6~~Figure 9-6~~~~Figure 9-6~~ and Figure 9-8~~Figure 9-8~~~~Figure 9-8~~ show, respectively, the low profile PCI Express add-in card form factor without and with the bracket, while Figure 9-9~~Figure 9-9~~~~Figure 9-9~~ shows the low profile add-in card I/O bracket. When mounting a low profile card into a full height PCI slot, the standard I/O bracket must be modified to add a stiffening flange. Figure 9-10~~Figure 9-10~~~~Figure 9-10~~ shows the modified full height I/O bracket for low profile cards.



CONFIGURATION	PRIMARY SIDE HEIGHT RESTRICTION
SINGLE SLOT	14.47 MAX [0.570]
DUAL SLOT	34.80 MAX [1.370]
TRIPLE SLOT	55.12 MAX [2.170]

A-0907

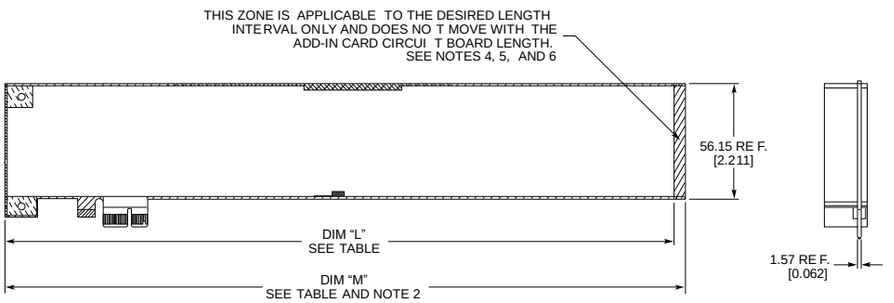
NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
2. THIS FEATURE IS TO PREVENT THE PCI EXPRESS CARD FROM BEING PLUGGED INTO PCI CONNECTORS.
3. THESE MOUNTING HOLES AND THE KEEP-OUT AROUND THEM ARE REQUIRED ONLY WHEN THE I/O BRACKET IS MOUNTED TO THE CARD DIRECTLY. FURTHERMORE, THESE ARE CHASSIS KEEPOUT AREAS, ARE INCLUDED IN THE ADD-IN CARD VOLUME, AND MUST ABIDE BY THE RESTRICTED COMPONENT HEIGHT, BOTH SIDES.
4. THESE MOUNTING HOLES MAY BE LOCATED DIFFERENTLY THAN AS SHOWN. ADDITIONALLY, THE SIZE OF THE KEEP-OUTS AROUND THESE HOLES ARE AT THE DISCRETION OF THE ADD-IN CARD PROVIDER.
5. CROSS HATCHED AREA REPRESENTS AN EXPOSED SIGNAL/POWER COMPONENT, FEATURE, AND TRACE FREE AREA, SECONDARY SIDE (SOLDER SIDE) ONLY. HOWEVER, NON-CONDUCTIVE FEATURES (PLASTIC LOCATION PINS, ETC.), GROUNDED FEATURES (BOARDLOCKS, GROUND PINS AND VIAS, ETC.) AND NON-EXPOSED TRACES ARE ALLOWED TO RESIDE IN THIS AREA.
6. CROSS HATCHED AREA REPRESENTS COMPONENT FREE AREA, BOTH SIDES.
7. NO COPPER OR SOLDER MASK IS ALLOWED IN CROSS HATCHED AREA, BOTH SIDES.
8. UNLESS OTHERWISE SPECIFIED AND ALONG "NORTH EDGE" ONLY, EXTERNALLY-MATED CONNECTORS, INCLUDING BUT NOT LIMITED TO POWER CONNECTORS, CARD-TO-CARD EDGE OR BRIDGE CONNECTORS, S/PDIF CONNECTORS, ETC. MAY ENCROACH INTO THIS AREA. INTRUSION BY SELF-CONTAINED COMPONENTS AND EXPOSED TRACES ARE PROHIBITED.
9. NO COMPONENTS OR SURFACE TRACES ALLOWED IN THIS AREA. IN ADDITION, ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO NOR ABOVE THE CARD EDGE IN THIS AREA. THIS KEEPOUT APPLIES TO BOTH SIDES OF THE CARD. THIS KEEPOUT ESTABLISHES A CONSISTENT REGION FOR SUPPLEMENTAL MECHANICAL SUPPORT OF THE ADD-IN CARD BY THE SYSTEM.

Figure 9-~~6~~9-~~6~~: Low Profile PCI Express Add-in Card without the I/O Bracket

Formatted: Font: 8 pt

Formatted: Indent: Left: 0", Space After: 0 pt, Line spacing: single



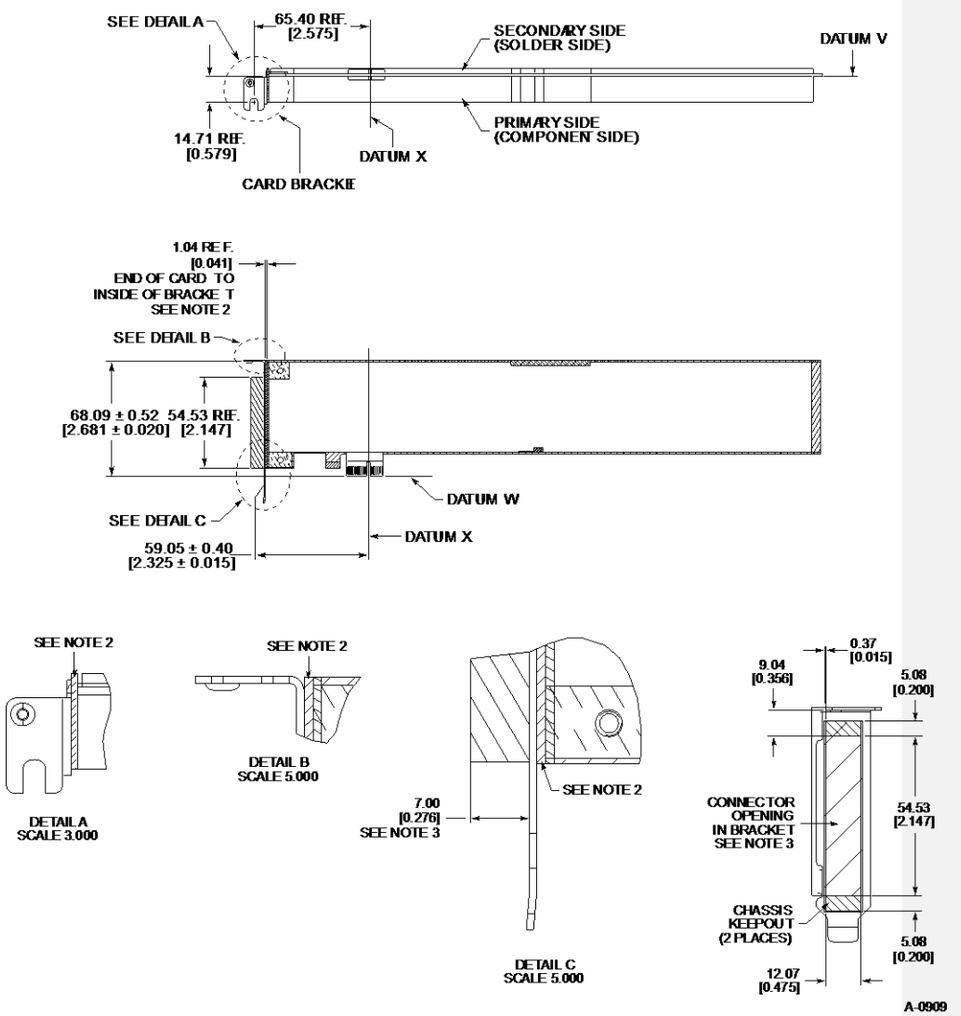
LENGTH INTERVAL	DIM "L"	DIM "M"
HALF LENGTH	166.65 [6.561]	167.65 MAX [6.600]
THREE-QUARTER LENGTH	248.92 [9.800]	254.00 MAX [10.00]
FULL LENGTH	306.92 [12.083]	312.00 MAX [12.283]

A-0908

NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
2. DIMENSIONS ESTABLISH A CONSISTENT VOLUME FOR END CARD MECHANICAL SUPPORT.
3. FOR EACH LENGTH INTERVAL, DIMENSION "M" ALSO DESCRIBES THE MAXIMUM OVERALL LENGTH OF THE ADD-IN CARD ASSEMBLY.
4. FOR EACH DESIRED LENGTH INTERVAL, FEATURES OF THE ADD-IN CARD ASSEMBLY MUST INTERSECT WITH THIS VOLUME. IF PART OF THE ADD-IN CARD CIRCUIT BOARD, THIS MUST BE A COMPONENT AND SURFACE TRACE FREE AREA, BOTH SIDES.
5. FOR EACH DESIRED LENGTH INTERVAL, SYSTEMS MUST ACCOMODATE THE ENTIRE DESCRIBED VOLUME OTHERWISE, ISSUES INCLUDING BUT NOT LIMITED TO NON-RETENTION OF ADD-IN CARD, FIT INTERFERENCE, ETC. COULD OCCUR.
6. FOR THE FULL LENGTH INTERVAL ONLY, ITEMS INCLUDING BUT NOT LIMITED TO HEATSINKS, DAUGHTER CARDS, OR MATING CONNECTORS (IN WHOLE OR IN PART) ARE NOT ALLOWED TO EXTEND INTO THIS AREA. THIS KEEPOUT APPLIES TO BOTH SIDES OF THE CARD. THESE ADDITIONAL COMPONENT AND TRACE RESTRICTIONS ARE DESIRED BUT NOT REQUIRED FOR THE HALF-LENGTH AND THREE QUARTER LENGTH INTERVALS.

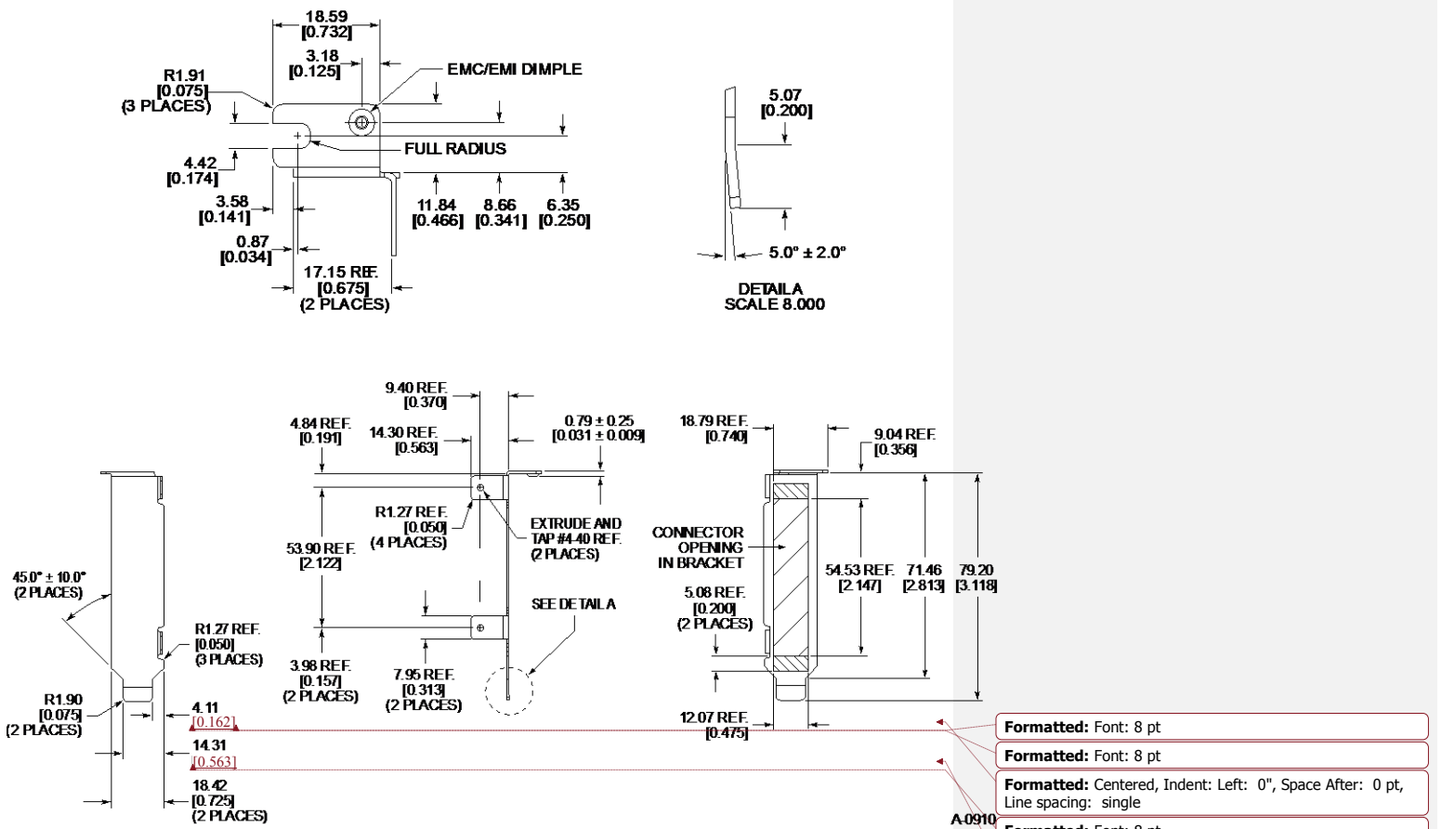
Figure 9-~~79~~ 7: Chassis Interface Zone on Right/East Edge of Low Profile Add-in Card



NOTES:

1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.13 [0.005]
2. INDICATED ZONE IS A SYSTEM NON-ENCROACH VOLUME, THROUGH ALL, BOTH SIDES.
3. THIS IS THE ALLOWABLE ZONE FOR CARD-MOUNTED CONNECTORS TO PROTRUDE THROUGH THE BRACKET. THIS DOES NOT INCLUDE MATING OR NON-PROTRUDING CONNECTORS.

Figure 9-~~8~~9 ~~8~~: Low Profile PCI Express Add-in Card with the I/O Bracket



NOTES:

1. MATERIAL: 0.86 ± 0.08 [0.034 ± 0.003] THICK (20 GA)
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.25 [± 0.010]

Figure 9-~~99~~ 9: Low Profile I/O Bracket

[0.162]

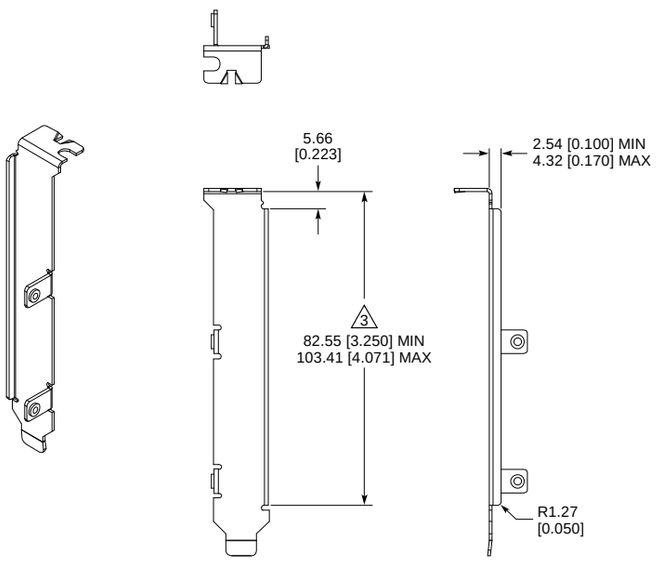
Formatted: Font: 8 pt

Formatted: Font: 8 pt

Formatted: Centered, Indent: Left: 0", Space After: 0 pt, Line spacing: single

Formatted: Font: 8 pt

Formatted: Centered, Indent: Left: 0", Space After: 0 pt, Line spacing: single



NOTES:
1. STIFFENING FLANGE IS REQUIRED WHEN MOUNTING A LOW PROFILE CARD TO A FULL HEIGHT BRACKET.

2. STIFFENING FLANGE IS OPTIONAL WHEN MOUNTING A FULL HEIGHT CARD.

3 THIS DIMENSION PROVIDES FOR CLEARANCE BETWEENTHE FLANGE AND COMPONENTS ON THE MOTHERBOARD.

4. THIS DRAWING SHOWS THE DIMENSIONS OF THE STIFFENING FLANGE ONLY. SEE FIGURE 9-5 FOR DIMENSIONS OF THE REMAINING FEATURES.

5. TOLERANCE UNLESS OTHERWISE NOTED: ± 0.25 [± 0.010]

A-0919

Figure 9-~~10~~ 10: Full Height I/O Bracket for Low Profile Cards

The form factor dimensions for a PCI Express DUAL-SLOT add-in card are shown in Figure 9-11~~Figure 9-11~~Figure 9-11.

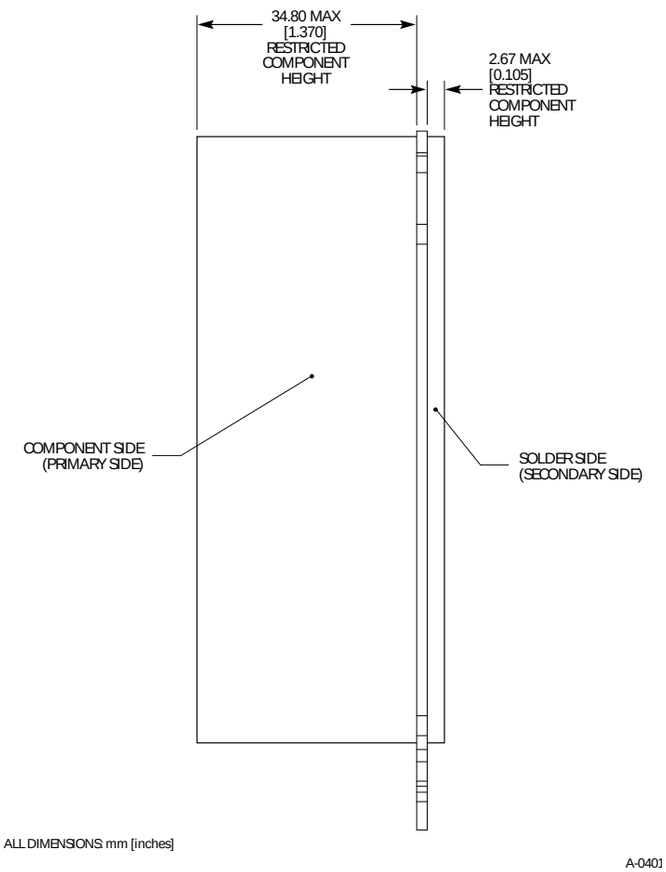


Figure 9-11~~9-11~~: PCI Express DUAL-SLOT Add-in Card Dimensional Drawing

The form factor dimensions for a PCI Express TRIPLE-SLOT add-in card are shown in Figure 9-12~~Figure 9-12~~Figure 9-12. The only difference from standard height full length cards is the additional spacing of the restricted component height on the primary side of the card.

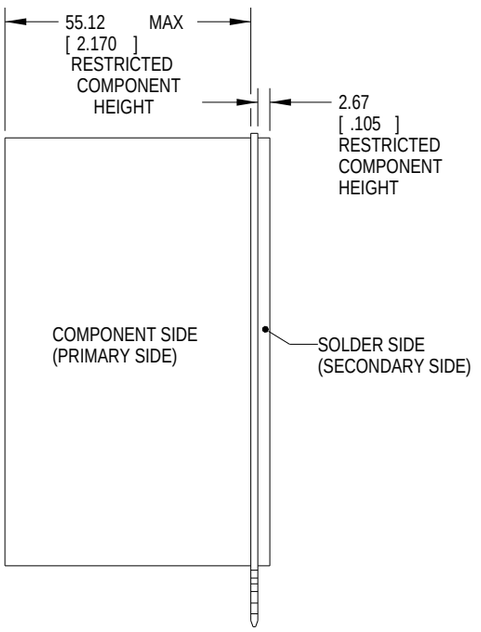


Figure 9-~~12~~9 ~~12~~: PCI Express TRIPLE-SLOT Add-in Card Dimensional Drawing

A PCI Express DUAL-SLOT add-in card may utilize a two slot I/O bracket to accommodate adequate thermal management.

Figure 9-13~~Figure 9-13~~Figure 9-13 is a detailed drawing of a two-slot I/O bracket design. Figure 9-14~~Figure 9-14~~Figure 9-14 is an isometric view of the two-slot I/O bracket with an area for graphics card venting. The size and number of any holes in the bracket follow proper EMI and thermal design guidelines.

Formatted: Do not check spelling or grammar

Formatted: Do not check spelling or grammar

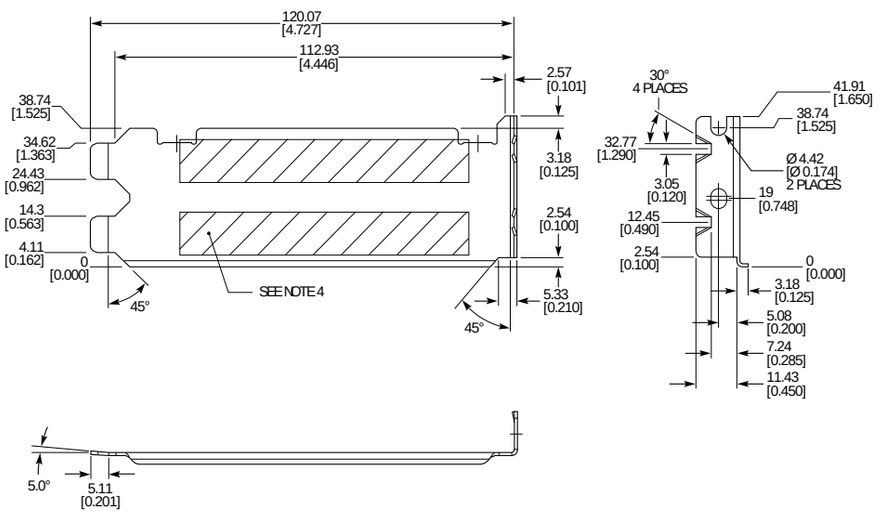


Figure 9-~~139~~ ~~13~~: Detailed Two-Slot I/O Bracket Design

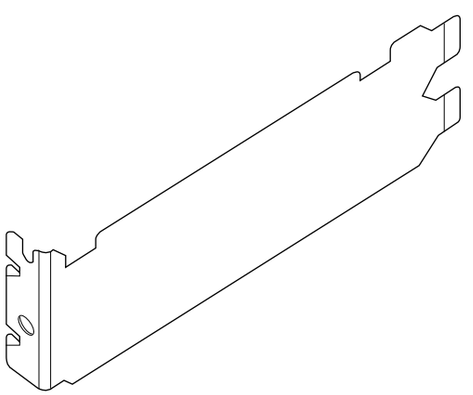
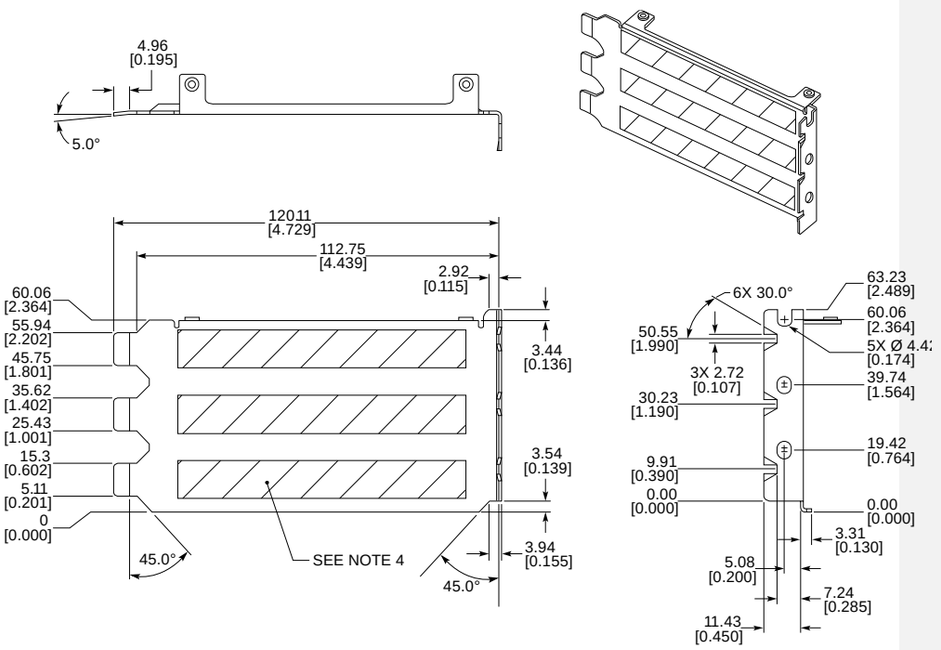


Figure 9-~~149~~ ~~14~~: Two-Slot I/O Bracket Example (Isometric View)

A PCI Express TRIPLE-SLOT add-in card may utilize a three slot I/O bracket to accommodate adequate thermal management.

Figure 9-15~~Figure 9-15~~Figure 9-15 is a detailed drawing of a three-slot I/O bracket design. Figure 9-16~~Figure 9-16~~Figure 9-16 is an isometric view of the three-slot I/O bracket with an area for graphics card venting. The size and number of any holes in the bracket follow proper EMI and thermal design guidelines.



NOTES:

1. MATERIAL: 0.034 THK (20 GA) LOW CARBON STEEL, ZINC PLATED.
2. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± 0.254 [0.010]
3. ALL DIMENSIONS: MM [INCHES].
4. CROSS HATCH AREA INDICATES I/O CONNECTOR/THERMAL VENTING WINDOW.

Figure 9-15~~9-15~~: Detailed Three-Slot I/O Bracket Design

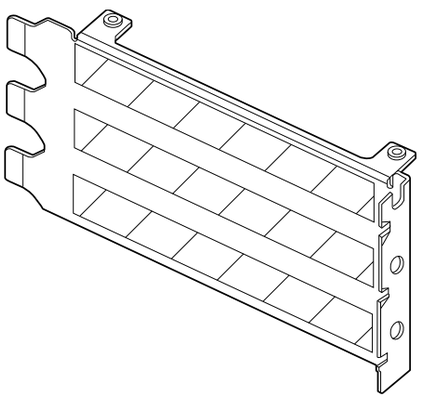


Figure 9-~~16~~9-~~16~~: Three-Slot I/O Bracket Example (Isometric View)

PCI Express add-in cards require additional card retention and support for cards that are greater than 350 grams in mass. Testing has shown that using the connector retention mechanism alone for cards over 350 grams will cause connector and/or card damage.

Additionally, use of the "hockey stick" retention feature defined in this specification with certain add-in card thermal solutions makes access to and disengagement of the connector retention mechanism difficult without special tools. As a result, the "hockey stick" feature is optional for a PCI Express add-in card.

IMPLEMENTATION NOTE

PCI Express Usage of the "Hockey Stick" Feature

~~As noted, t~~The hockey stick feature is optional for a PCI Express add-in card design. The actual board design used to omit this feature is implementation dependent, but the resultant layout cannot exceed any CEM outline measurement.

This specification defines keepouts and features on any PCI Express add-in card to be used for card retention. Detailed retention mechanism design, however, is considered implementation specific and it is up to system OEMs to work with card vendors.

The following guidelines should be observed when designing retention mechanism for high mass add-in cards:

The use of the "hockey stick" feature alone is unlikely to be sufficient because of the high card mass allowed in this specification (1.5 kg maximum). The use of the keepout area to hold the card in place is strongly recommended. This mechanism may be necessary to prevent excessive deformation of the card during shock and vibration.

The bracket is part of the card retention mechanism. It should have sufficient mechanical strength to withstand system-level shock and vibration. Deformation of card brackets has been one of the major failure mechanisms in the past.

Formatted: Font: (Default) Arial, 11 pt, Bold

Formatted: Space Before: 3 pt, After: 0 pt

Formatted: Font: (Default) Arial, 10 pt

Formatted: Space After: 3 pt

Formatted: Font: 10 pt

Formatted: Font: (Default) Arial, 10 pt

All cards shall be enabled for a full-length add-in card retainer. Partial length cards shall have means of being extended to full length and equipped with the retainer. The card features used for extending partial length cards to full length are the card vendor's option; they may include component keep-outs and holes similar to those shown in Figure 9-1~~Figure 9-1~~~~Figure 9-1~~.

All cards shall be enabled for a full-length stiffener to minimize card flexure during dynamic events. When included, the stiffener should be located within the card component keep-in volume as defined in Figure 9-11~~Figure 9-11~~~~Figure 9-11~~ and Figure 9-12~~Figure 9-12~~~~Figure 9-12~~. Implementation details are the card vendor's option.

A PCI Express card shall not exceed 1.5 kilograms in mass. To support such a mass, attentions must be paid to bracket, chassis strengths, and retention mechanism designs. Card manufacturers should make efforts to minimize the card mass.

9.2. Add-in Card Layout Requirements and Recommendations for 16 GT/s Operation

Operating at a data rate of 16 GT/s places additional requirements on the add-in card layout specifically with respect to the ~~edge finger~~edge-fingers. ~~The following guidelines are required except where explicitly stated as optional but recommended~~.

9.2.1. Void Under All ~~Edge Finger~~Edge-fingers

There shall be no conductors of any kind, ~~specifically~~such as ground or power planes, underneath the ~~edge finger~~edge-fingers. Any conductors in this region increase capacitance with respect to the high speed signal lines increasing insertion loss and crosstalk.

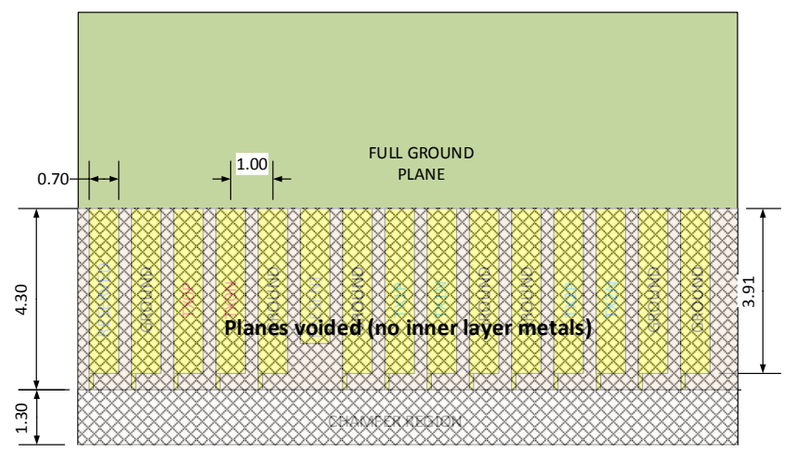


Figure 9-17: Add-in Card ~~Edge Finger~~Edge-fingers Indicating Void Under ~~Edge Finger~~Edge-fingers

Formatted: Font color: Auto
Formatted: Font color: Auto
Formatted: Font color: Gray-80%
Formatted: Indent: Left: 0", Hanging: 0.9"
Formatted: Indent: Left: 0", Hanging: 0.9", Space After: 6 pt
Formatted: Keep with next
Formatted: FigureTitle, Don't suppress line numbers

9.2.2. No Missing ~~Edge Finger~~Edge-fingers

~~In some implementations at lower data rates, unused connections (usually reserved side band signals but occationally, ground connections) have the edge finger completely missing. This causes significant crosstalk problems at 16 GT/s so it cannot be done at this data rate.~~ Unused Edge-fingers can not be removed from the card edge.

9.2.3. ~~Edge Finger~~Edge-finger Length

~~Edge finger~~Edge-fingers ~~should be~~are 3.91 mm (154.0 mil) in length with the top of the ~~edge finger~~edge-finger located 5.59 mm (220.0 mil) (above the bottom edge of the add-in card ~~edge finger~~edge-finger region). This i~~m~~proves the crosstalk performance of the high speed signal lines and reduces problems caused by burrs created during the chamfer operation.

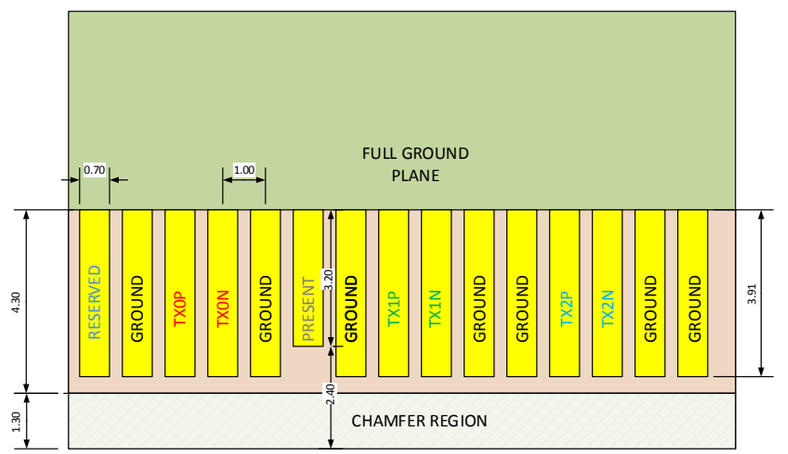


Figure 9-~~18~~: Add-in Card ~~Edge Finger~~Edge-fingers Indicating Correct ~~Edge Finger~~Edge-finger Length

9.2.4. Lowered ~~Edge Finger~~Edge-finger Ground Vias

~~Many add-in cards have up to 2.0 mm (78.7 mil) of trace from the ground edge fingers to the ground via location. This allows a resonance condition which reduces performance above 8 GT/s. Moving the ground via to be at the top of the edge finger (offset to the left or right to avoid blocking the escape from adjacent signal conductors) moves the resonance higher in frequency thus moving it above the 16 GT/s signaling range.~~ Ground vias ~~wi~~shall be located centrally between the two edge-fingers. Ground vias shall be located no more then 15mils from the top of the edge-finger.

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Keep with next

Formatted: FigureTitle, Don't suppress line numbers

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

Commented [NM11]: Reword? Refine

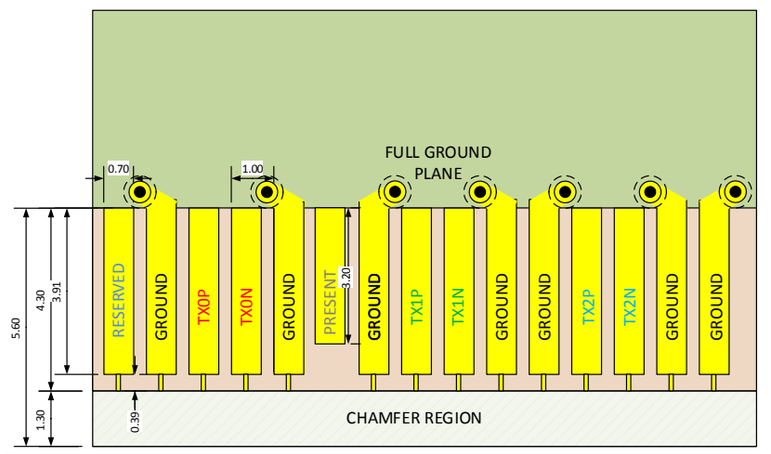


Figure 9-19: Add-in Card ~~Edge Finger~~Edge-fingers Indicating Lowered Ground Vias

9.2.5. Joined ~~Edge Finger~~Edge-finger Ground Vias

Many of the ground ~~edge finger~~edge-fingers are double grounds (two ground edgefingers adjscent to each other). In these cases, joining the adjscent ~~edge finger~~edge-fingers at the lowered via location is required as this provides significant additional improvement in the ground resonance. Lowered ground vias can also be shared by ground ~~edge finger~~edge-fingers on opposing sides of the add-in card.

Formatted: Keep with next

Formatted: FigureTitle, Don't suppress line numbers

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

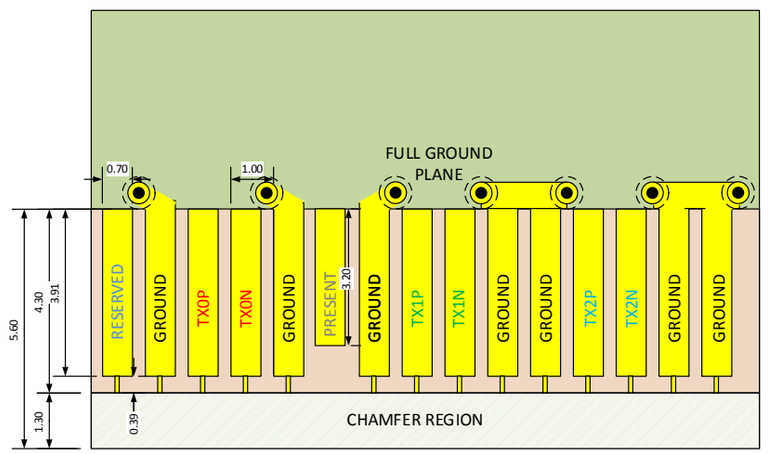


Figure 9-20: Add-in Card ~~Edge Finger~~Edge-fingers Indicating Lowered and Joined Ground Vias

9.2.6. Auxiliary Signal Conductor Termination

On the high speed section of the add-in card edge-finger region (at and above pin 12) there are several auxiliary signals which are either used (such as CLKREQ#, PWRBRK# and PRSNT2#) or unused (RESERVED). In all cases, leaving these pins unterminated allows the conductive structure (from system board through the connector via and connector to the add-card ~~edge finger~~edge-finger) to act as resonator that takes energy from one pair of high frequency data lines and radiates this energy to another pair of high frequency data lines. This causes a surprising amount of crosstalk at roughly 4.6 GHz.

Terminating these conductors through a 43.5 Ω impedance to ground essentially eliminates this resonance and the resulting high frequency crosstalk. In order to avoid compromising any low frequency signaling on these auxiliary conductors (such as referenced above) a DC blocking capacitor must be added to the termination. To accomplish the required termination, all conductors carrying auxiliary signals shall be terminated by an appropriate resistance (nomally 43.5 Ω) in series with an appropriate capacitance (nomally 1.0 pF) to ground. This is required for add-in cards and recommended for system boards.

A X1 add-in card or connector requires four auxiliary signals be terminated, CLKREQ# (B12), REFCLK+ (A13), REFCLK- (A14), PRSNT2# (B17). A X4 card or connector requires four more terminations, RSVD (A19 and A32), PWRBRK# (B30), PRSNT2# (B31). A X8 card or connector requires two more terminations, RSVD (A50), PRSNT2# (B81). A X16 card or connector also requires two more terminations, RSVD (A50), PRSNT2# (B81).

The trace length from the top of an auxiliary signal edge-finger to the termination components should be as short as practicable and should never exceed 500 mil.

Formatted: Keep with next

Formatted: FigureTitle, Don't suppress line numbers

Commented [NM12]: Change to required
Explicitly list theAux signals/pin#

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

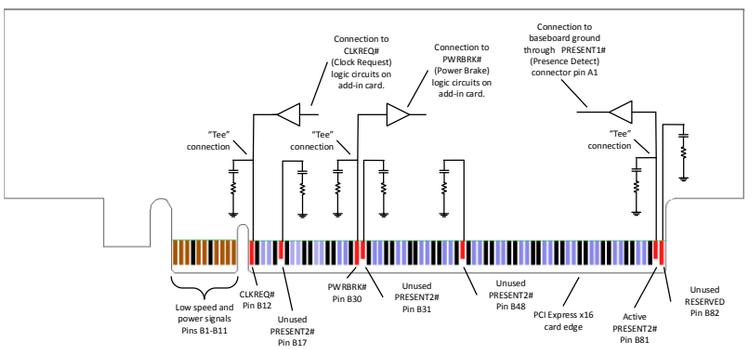


Figure 9-21: Add-in Card with AC Terminations on All Auxiliary Signal Conductors

9.3. System Board Re~~commendations~~quirements for 16 GT/s Operation

The system board can be updated to improve operation at 16 GT/s as well. ~~These guidelines are recommended but not required.~~ Adding these layout optimizations to the system board are completely compatible with all add-in card ~~required and recommenced~~ optimizations so there is no chance for a conflict with system board optimizations and add-in card optimizations.

~~Auxiliary Signal Conductor Termination (Recommended But Not Required)~~

~~auxiliary conductor terminations as discussed in section 9.2.6 above can be added to auxiliary signal conductors on the system board. These high frequency terminations provide additional reduction for crosstalk caused by auxiliary signal conductors.~~

Formatted: figure, Don't suppress line numbers

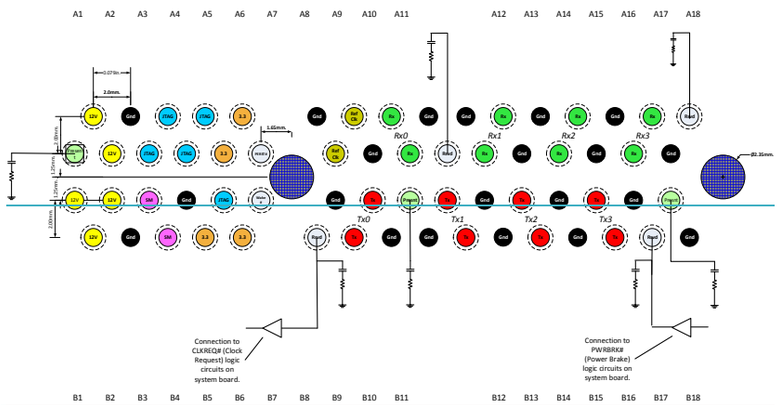
Formatted: Check spelling and grammar

Formatted: Heading 2,Section Name,H2,H21,H22,H211,H23,H212,H24,H213,H25,H214,H26,H215,H27,H216,H28,H217,H221,H2111,H231,H2121,H241,H2131,H251,H2141,H261,H2151,H271,H2161,H29,H218,H222,H2112,H232,H2122,H242,H2132,H252,H2142,H262,H2152,H272,H2162,H210,H219,H223,H233, Indent: Left: 0", Hanging: 0.9", Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers



Formatted: Keep with next

~~Figure 9-22: System Board with AC Terminations on All Auxiliary Signal Conductors~~

Formatted: FigureTitle, Space After: 0 pt, Don't keep with next

9.3.1. "Sentry Vias" Applied to All Auxiliary Signal Vias

Commented [NM13]: Add specific list of signals
Excact placement and other rules for placement of these vias TBD for 0.5-add a note mentioning this

Add a note saying this requirement is only for vias that exist

"Sentry Vias" are minimum diameter (10 mil, 8 mil or what ever minimum diameter via the board fabricator can economically provide) ground vias that are placed adjscent to any auxiliary signal vias on the system board. From two to four vias ~~can~~shall be used for each auxiliary signal via.

Formatted: Heading 3,Sub-section name,H3, Indent: Left: 0", Hanging: 0.9", Space After: 6 pt, Don't suppress line numbers

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

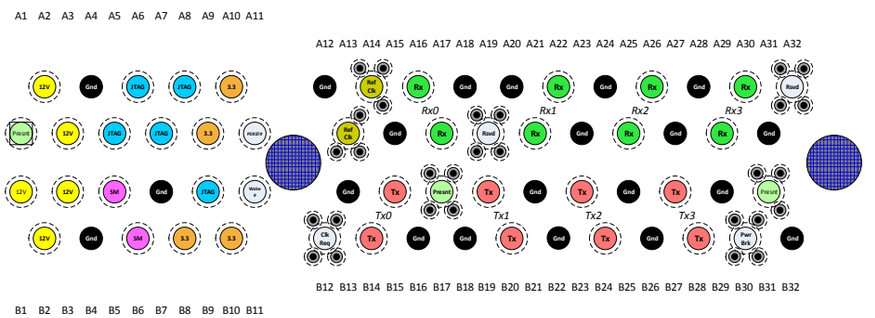


Figure 9-~~2223~~: System Board with Sentry Vias on All Auxiliary Connector Vias

Formatted: FigureTitle, Don't suppress line numbers

When a surface mount connector or straddle mount connector is used, only auxiliary signals that have a via near any high speed data signal vias are required to isolate the auxiliary signal via with Sentry vias.

Formatted: Not Highlight

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

A X1 connector requires four auxiliary signals be isolated with Sentry vias, CLKREQ# (B12), REFCLK+ (A13), REFCLK- (A14), PRSNT2# (B17). A X4 connector requires four more auxiliary signals be isolated, RSVD (A19 and A32), PWRBRK# (B30), PRSNT2# (B31). A X8 connector requires two more auxiliary signls be isolated, RSVD (A50), PRSNT2# (B81). A X16 connector also requires two more auxiliary signals be isolated, RSVD (A50), PRSNT2# (B81).

Formatted: Not Highlight

Formatted: Normal, Space After: 6 pt, Don't suppress line numbers

~~9.2.~~9.4. Connector and Add-in Card Locations

Figure 9-23~~Figure 9-24~~~~Figure 9-17~~ shows an example of a typical desktop system (microATX form factor). The add-in card slots are occupied by the PCI and AGP add-in card connectors.

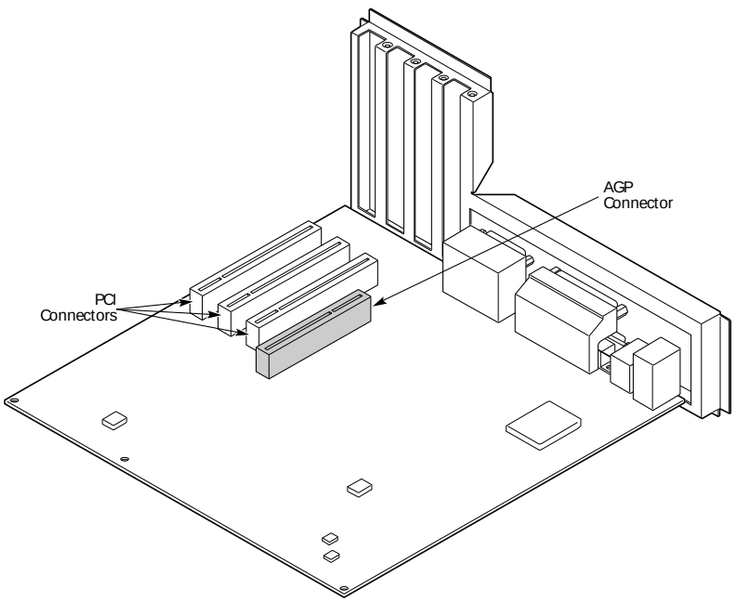


Figure 9-~~23249-17~~: Example of a PC System in microATX Form Factor

The PCI Express add-in cards will use the space allocated for those add-in card slots to take advantage of the existing chassis infrastructure. This requirement dictates that the PCI Express connectors must use the slots that coincide with the locations of the present PCI and AGP slots/connectors.

Figure 9-24~~Figure 9-25~~~~Figure 9-18~~ illustrates the introduction of a PCI Express connector in a microATX system, co-existing with the PCI connectors. In this case, the PCI Express connector is introduced by replacing the AGP connector.

Like the PCI add-in card, the components on a PCI Express add-in card face away from the CPU, or the core area.

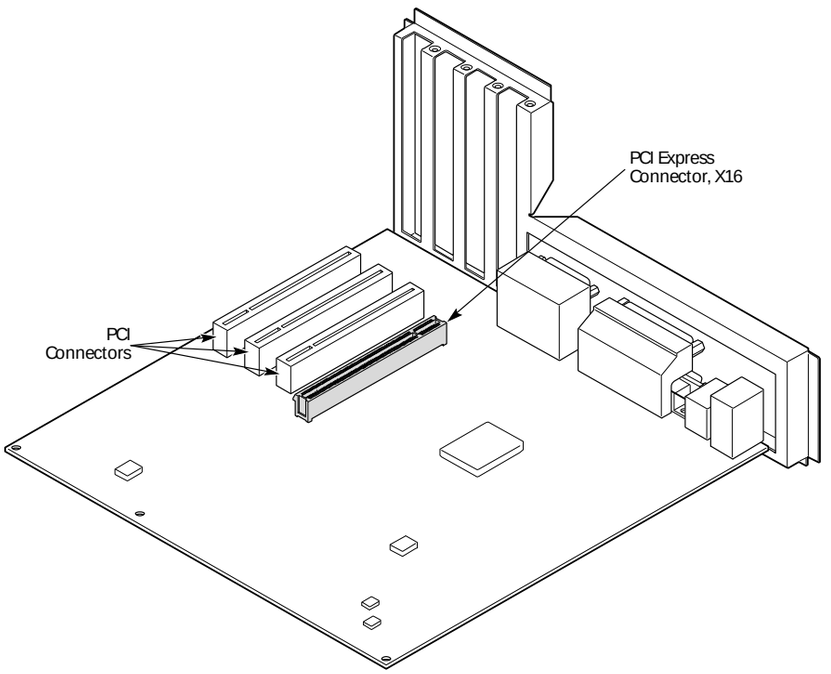


Figure 9-~~24259-18~~: Introduction of a PCI Express Connector in a microATX System

Over time, more PCI Express connectors will be used on the system board. Figure 9-25~~Figure 9-26~~~~Figure 9-19~~ shows a situation in which a basic bandwidth PCI Express connector replaces a PCI connector (x1) and a high bandwidth (x16) PCI Express connector replaces the AGP connector.

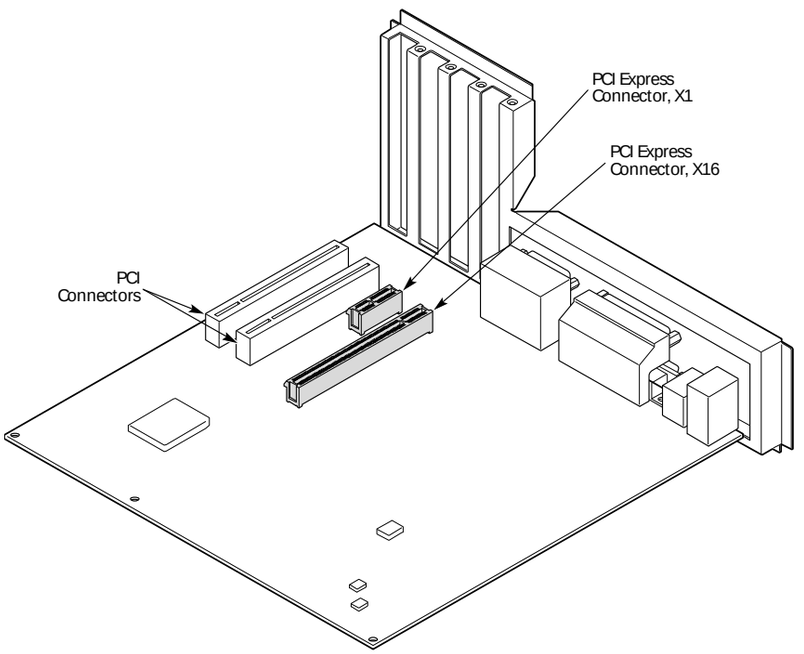


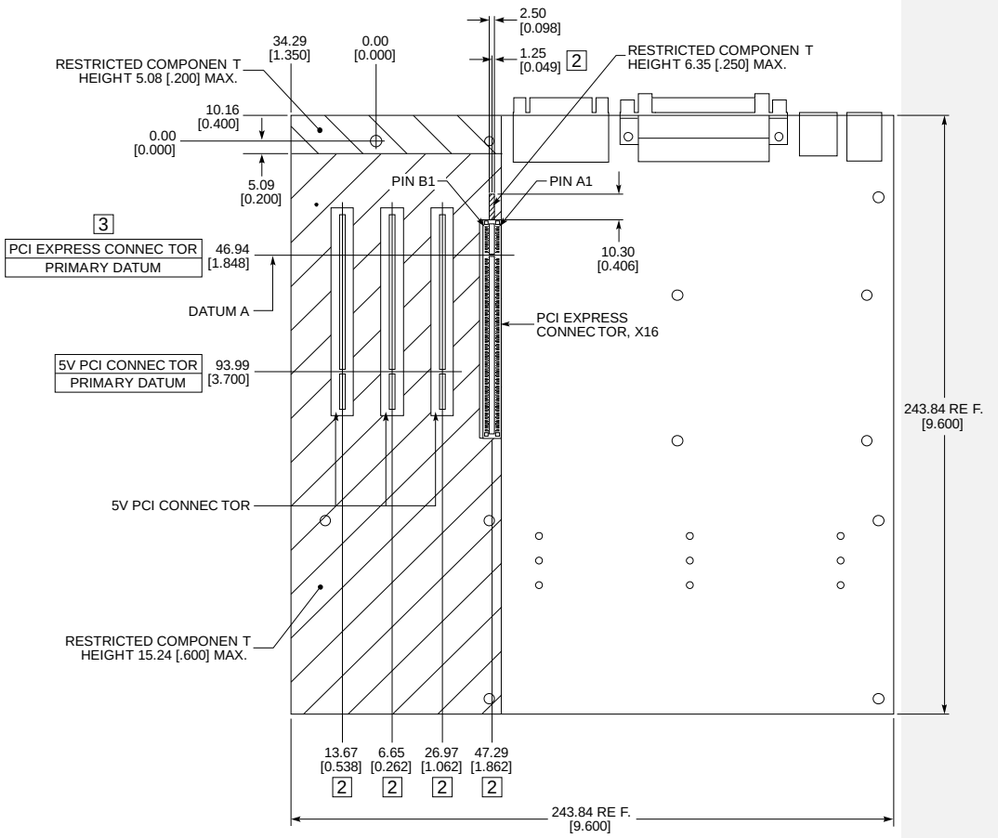
Figure 9-~~25269-19~~: More PCI Express Connectors are Introduced on a microATX System Board

Figure 9-26~~Figure 9-27~~~~Figure 9-20~~ shows the PCI Express connector location, as well as the component height restriction zones. In this case, a x16 PCI Express connector replaces the AGP connector. When more PCI Express connectors are introduced, the height restriction zones will grow accordingly. This is depicted in Figure 9-27~~Figure 9-28~~~~Figure 9-21~~, where an additional x1 PCI Express connector is introduced along with the x16 connector. The 5.08 ~~-~~mm (0.~~200~~ 200 inches) maximum and the 15.24 ~~-~~mm (0.~~600~~ 600 inches) maximum height restriction zones are identical to the PCI requirements. But the additional, small height restriction zones of 6.~~35~~ 35 mm (0.~~250~~ 250 inches) max are unique to PCI Express.

There is a slight offset between PCI and PCI Express connector locations. The PCI Express connectors are located slightly further away from the rear of the chassis. The PCI Express add-in cards contain features (see Note 2 in Figure 9-1~~Figure 9-1~~~~Figure 9-1~~ and Figure 9-6~~Figure 9-6~~~~Figure~~

~~9-6~~) to prevent them from being mistakenly inserted into a PCI slot. Such features require the additional height restriction zones of 6.~~35~~ 35 mm (0.~~250~~ 250 inches) maximum.

The card retention clip may require additional height restrictions. Such restrictions depend on the retention clip design and location, which may vary from user to user. Thus, they are not specified here as a requirement. However, in the design guideline, a reference retention clip design and implementation is given, together with the keep-out and height restriction zones.



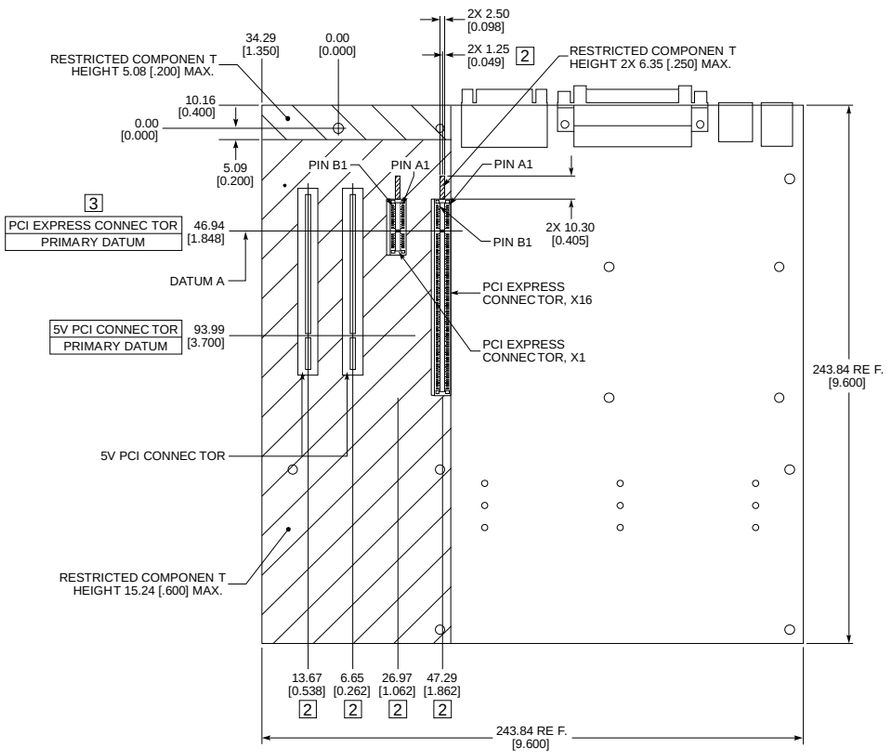
NOTES:
1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± .25 [± .010]

2 CENTER LINE OF CONNECTOR.

3 THE PRIMARY DATUM IS THE DATUM –A– ON THE CONNECTOR (SEE FIGURE 6-1).

A-0913

Figure 9-26279-20: PCI Express Connector Location in a microATX System with One PCI Express Connector



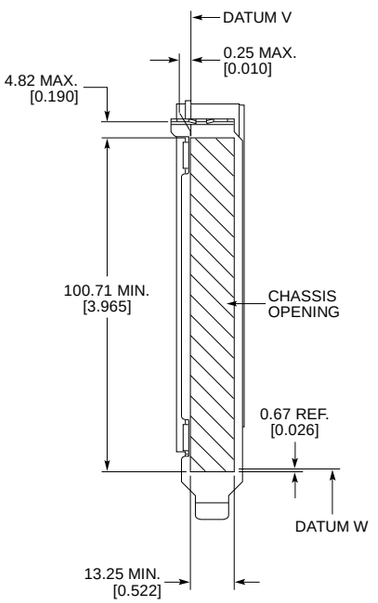
NOTES:
1. TOLERANCE UNLESS OTHERWISE SPECIFIED: ± .25 [± .010]

2 CENTER LINE OF CONNECTOR.

3 THE PRIMARY DATUM IS THE DATUM –A– ON THE CONNECTOR (SEE FIGURE 6-1).

A-0914

Figure 9-~~27289-21~~: PCI Express Connector Location in a microATX System with Two PCI Express Connectors



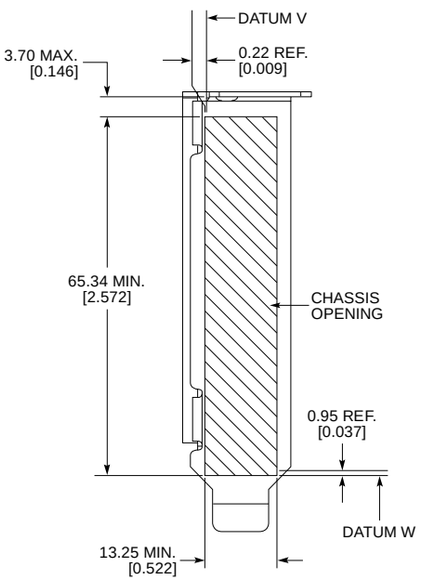
NOTES:
1. CHASSIS OPENING IS THE MINIMUM REQUIRED APERTURE, TAKING INTO ACCOUNT REFERENCE SYSTEM LEVEL TOLERANCES. ACTUAL DIMENSIONS WILL VARY BASED ON SYSTEM IMPLEMENTATION.

2. THE SIZE OF THIS CHASSIS OPENING MUST INCLUDE SYSTEM ACCOMODATIONS, INCLUDING BUT NOT LIMITED TO: PROTRUDING CONNECTORS ON THE ADD-IN CARD, INSERTION AND REMOVAL OF THE ADD-IN CARD FROM THE SYSTEM, ETC.

3. I/O CONNECTORS MATING TO THE CARD CAN HAVE OVERMOLDS EXTENDING IN ALL DIRECTIONS AROUND THIS OPENING. THIS WILL LIMIT THE EFFECTIVE THICKNESS OF THE CHASSIS NEAR THIS REGION.

A-0915

Figure 9-~~28299-22~~: Standard Height Connector Opening in Chassis



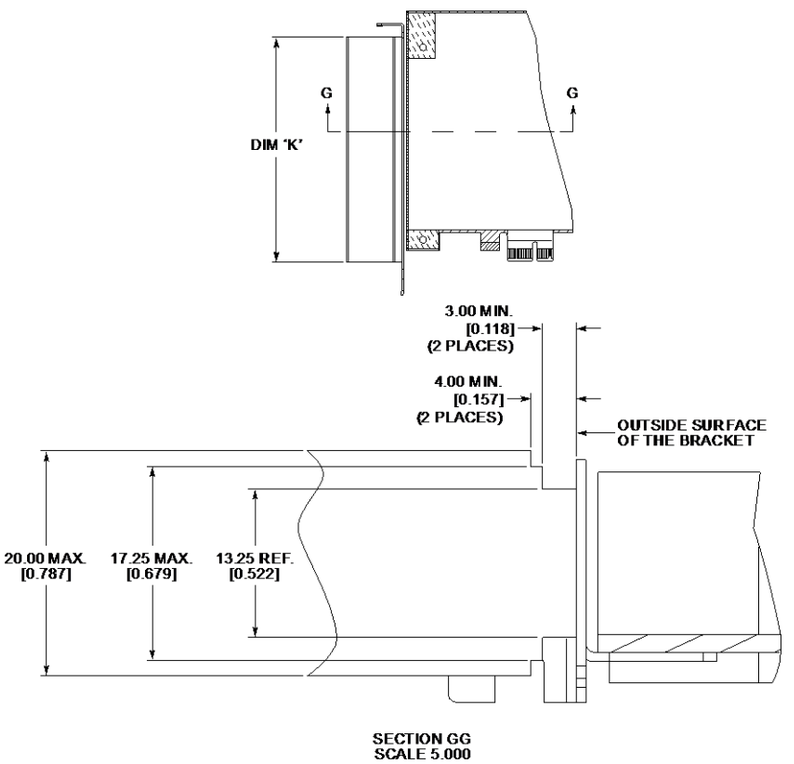
NOTES:
1. CHASSIS OPENING IS THE MINIMUM REQUIRED APERTURE, TAKING INTO ACCOUNT REFERENCE SYSTEM LEVEL TOLERANCES. ACTUAL DIMENSIONS WILL VARY BASED ON SYSTEM IMPLEMENTATION.

2. THE SIZE OF THIS CHASSIS OPENING MUST INCLUDE SYSTEM ACCOMODATIONS, INCLUDING BUT NOT LIMITED TO: PROTRUDING CONNECTORS ON THE ADD-IN CARD, INSERTION AND REMOVAL OF THE ADD-IN CARD FROM THE SYSTEM, ETC.

3. I/O CONNECTORS MATING TO THE CARD CAN HAVE OVERMOLDS EXTENDING IN ALL DIRECTIONS AROUND THIS OPENING. THIS WILL LIMIT THE EFFECTIVE THICKNESS OF THE CHASSIS NEAR THIS REGION.

A-0916

Figure 9-~~29309-23~~: Low Profile Connector Opening in Chassis



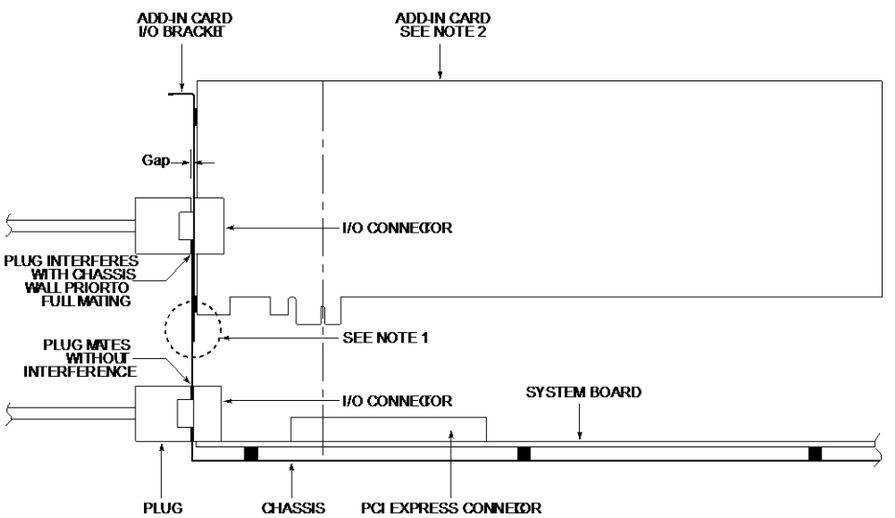
CARD HEIGHT	DIM 'K'
STANDARD HEIGHT (SEE FIGURE 9-22)	100.71 REF. [3.965]
LOW PROFILE (SEE FIGURE 9-23)	65.34 REF. [2.572]

A-0917

NOTES:

1. THE VOLUMETRIC CHASSIS KEEPOUT SHOWN REPRESENTS THE CLEARANCE REQUIRED TO ENABLE FULL MATING OF CABLE ASSEMBLIES TO I/O CONNECTORS ON THE ADD-IN CARD.
2. THE DESCRIBED VOLUME IS THE MINIMUM REQUIRED. ACTUAL DIMENSIONS WILL VARY BASED ON SYSTEM IMPLEMENTATION.

Figure 9-~~30319-24~~: Chassis I/O Cable Keepout



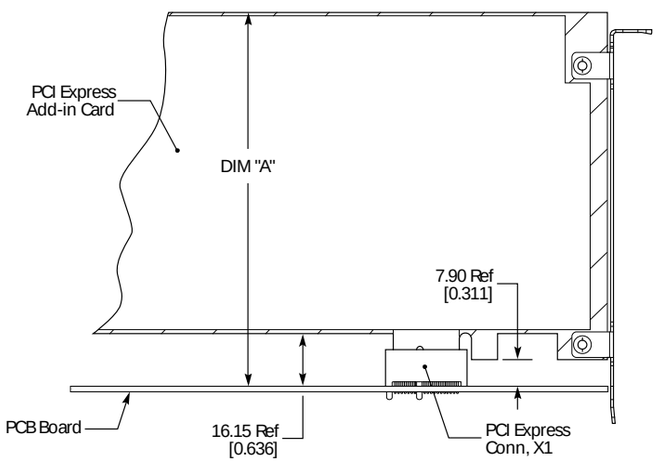
NOTES:
1. AS THE ADD-IN CARD BRACKET RESIDES BEHIND THE CHASSIS WALL WHEN INSTALLED IN THE SYSTEM BOARD CONNECTOR, THE RESULTING DOUBLE WALL THICKNESS REDUCES THE PROTRUSION OF THE I/O CONNECTOR SUCH THAT THE CABLE PLUG MAY NOT FULLY MATE. SEE FIGURES 9-22 AND 9-23 FOR MINIMUM CHASSIS CLEARANCE GUIDANCE. SEE ALSO FIGURE 9-24 FOR CHASSIS KEEPOUT/CABLE + PLUG KEEP-IN VOLUMETRIC DEFINITION.
2. ADDITIONAL TOLERANCE FROM OTHER SOURCES (PCI EXPRESS CONNECTOR-TO-SYSTEM BOARD, ETC.) CAN FURTHER PREVENT THE CABLE + PLUG FROM MATING FULLY TO AN ADD-IN CARD I/O CONNECTOR.
3. ADD-IN CARDS ARE UNIVERSAL. THEREFORE, ADD-IN CARD DESIGNERS MUST ASSUME THAT ADEQUATE CLEARANCE FOR I/O MATING CABLE PLUGS WILL BE PROVIDED IN THE SYSTEM. SEE FIGURES 9-22, 9-23, AND 9-24 FOR ADDITIONAL DETAILS ON THE NEEDED CLEARANCES.

A-0918

Figure 9-~~31329-25~~: Impact of Structural Shapes in the System

Figure 9-31~~Figure 9-32~~~~Figure 9-25~~ shows examples of structure shapes that could affect cable attachment. Chassis wall thickness greater than the ATX wall thickness as well as the use of structural shapes formed in the chassis wall between slots as shown may also affect cable attach.

Figure 9-32~~Figure 9-33~~~~Figure 9-26~~ shows the card height with respect to the top surface of the system board when assembled into a connector.



DIM "A"	
STANDARD HEIGHT	114.55 [4.510] MAX.
LOW PROFILE	72.30 [2.846] MAX.

OM14767

Figure 9-32~~39 26~~: Card Assembled in Connector

9.3.9.5. Card Interoperability

PCI Express cards and connectors exist with a variety of Link widths. The interoperability of cards and connectors is summarized in Table 9-2~~Table 9-2~~~~Table 9-2~~.

Table 9-2~~9-2~~: Card Interoperability

Connector / Card	x1	X4	X8	x16
x1	Required	Required	Required	Required
x4	No	Required	Required	Required
x8	No	No	Required	Required
x16	No	No	No	Required

~~Note that t~~The connectors here refer to the receptacle connectors mounted on a system board, as defined in Chapter 5. The shaded area above the diagonal of Table 9-2~~Table 9-2~~~~Table 9-2~~ represents up-plugging, while the area below the diagonal represents down-plugging. ~~The~~ Be aware of the~~following points should be noted~~:

- Down-plugging, i.e., plugging a larger edge size card into a smaller connector, is not allowed and is physically prevented.
- Up-plugging, i.e., plugging a smaller edge size card into a larger connector, is supported.
- All PCI Express add-in cards must be able to negotiate and operate in all smaller Link widths from the full Link width down to x1. The x2 and x12 Link widths are optional.
- The upstream PCI Express components on a system board must be able to negotiate and operate in all smaller Link widths from the full Link width down to x1. The x2 and x12 Link widths are optional.

~~9.4.~~9.6. 150 W Thermal Management

Increasing power has a corresponding impact on the thermal management solutions of both the PCI Express 150 W add-in card and the platforms that support them. To guarantee robust system operation and reliability, the card and system must work together to dissipate the additional thermal load the 150 W add-in card puts on the system. It is recommended that the card manage its exhaust flow with respect to the system enclosure. For most ATX systems, it is recommended that the card exhaust heat to the outside of the system enclosure. This type of card thermal solution has the least impact on systems that use typical ATX chassis designs.

For other 150 W add-in card thermal designs, it is recommended that the card manufacturer and chassis designer or system integrator work closely together to insure the card, chassis, and system components work together so that performance and component reliability are not impacted.

Formatted: Not Highlight

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

10

10. PCI Express ~~225~~ 225 W/~~300~~ 300 W Add-in Card Thermal and Acoustic Management

Increasing card power has a corresponding impact on the thermal (for example, inlet temperature and airflow) and acoustic management solutions of the PCI Express ~~225~~ 225 W/~~300~~ 300 W high power add-in cards and the platforms that support them. To ensure robust system operation and reliability, the high power cards and systems must work together to dissipate the additional thermal load the card puts on the system.

10.1. Inlet Temperature

Inlet temperature is defined as the average temperature at the card thermal solution's fan inlet. Since the fan location may vary for different cards, engineering judgment should be utilized to determine the exact locations for the inlet temperature sensors placement. Figure 10-1~~Figure 10-1~~ illustrates an example showing the temperature sensor placement at the thermal solution inlet; one may consider the averaged temperature measured by the different sensors as the inlet temperature.

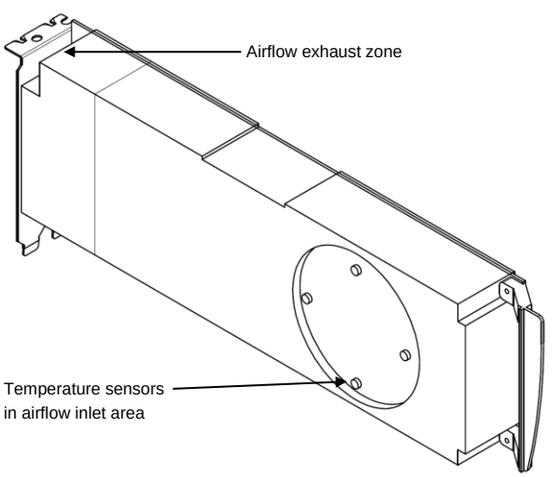


Figure 10-~~1~~10-1: Example of High-Power Card Showing Temperature Sensor Placements at the Thermal Solution Inlet

The procedure described in Section 10.2 should be used as a guideline for characterizing the high power add-in card. The add-in card inlet temperature should be controlled at 45 °C for both ~~300~~ 300 W and ~~225~~ 225 W cards.

For cards with a forced convection thermal solution, the rear bracket shall include vents for airflow exhaust to the outside of the system. Any airflow exhaust inside the system should be located at the rear end of the card as shown in Figure 10-1~~Figure 10-1~~~~Figure 10-1~~. It is recommended that any airflow exhaust inside the system should be located within 2.0 inches of the rear bracket.

10.2. Card Thermal Characterization Procedure

The following method should be used to carry out thermal characterization of ~~225~~ 225 W/~~300~~ 300 W high power add-in card:

The measurement should be carried out on a ~~225~~ 225 W/~~300~~ 300 W high-power add-in card with an open bench test setup system as shown in Figure 10-2~~Figure 10-2~~~~Figure 10-2~~ to Figure 10-4~~Figure 10-4~~~~Figure 10-4~~. Figure 10-2~~Figure 10-2~~~~Figure 10-2~~ illustrates a setup to test a DUAL-SLOT card. ~~Note that d~~Dimensions in Figure 10-2~~Figure 10-2~~~~Figure 10-2~~ apply to other fixture versions shown in Figure 10-3~~Figure 10-3~~~~Figure 10-3~~ and Figure 10-4~~Figure 10-4~~~~Figure 10-4~~, except ~~as noted~~where indicated otherwise. The fixture may be made of ¼ inch thick polycarbonate plastics, simulating full-length adjacent cards and a standard rear chassis panel.

Formatted: Not Highlight

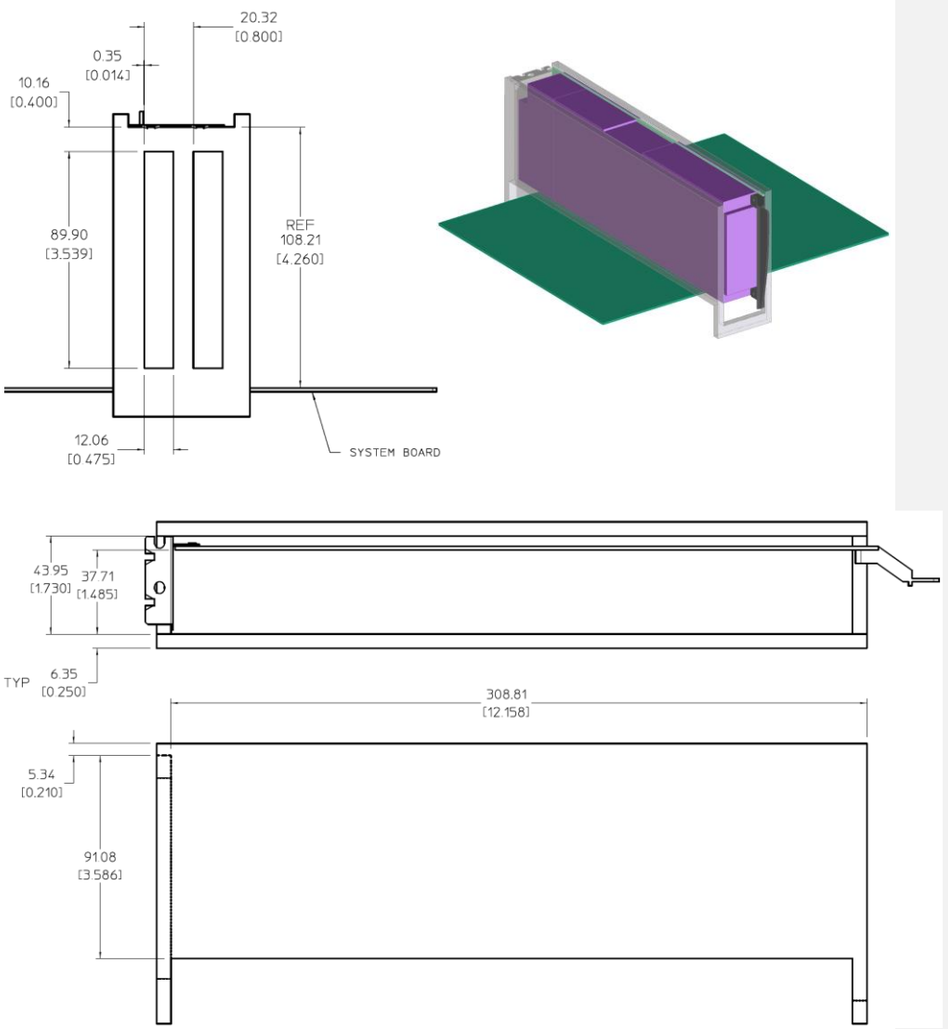


Figure 10-~~210-~~2: Thermal Characterization Fixture – DUAL-SLOT Version

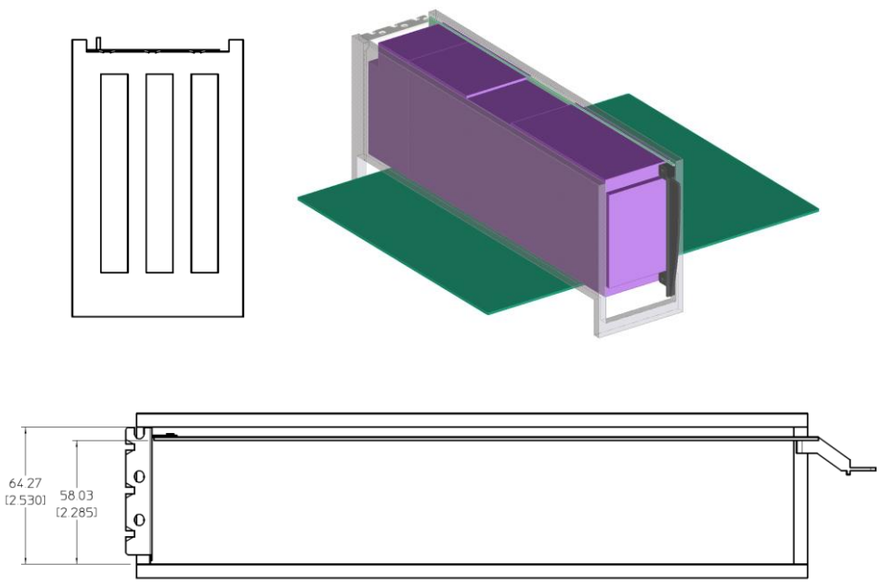


Figure 10-~~3~~10-~~3~~: Thermal Characterization Fixture – TRIPLE-SLOT Version

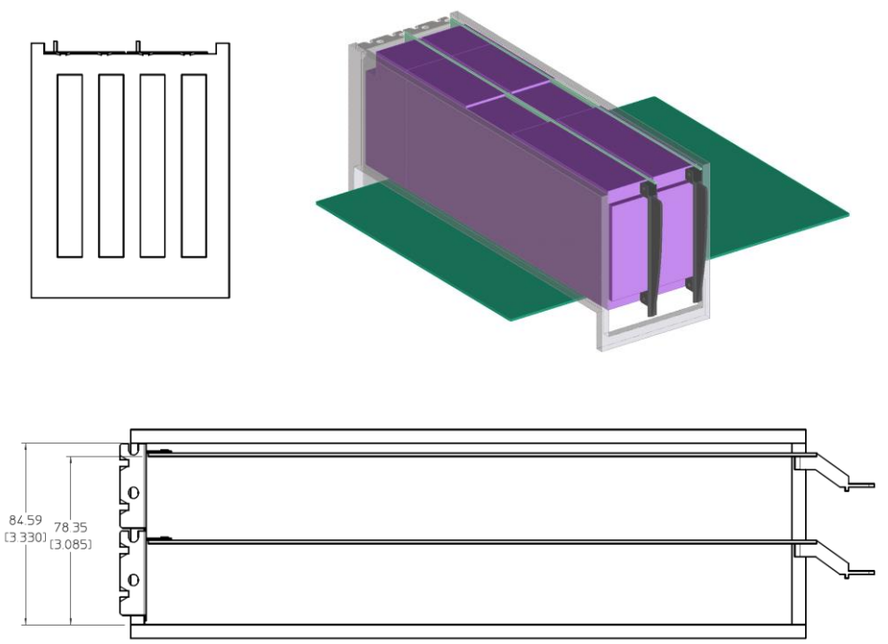


Figure 10-~~410-4~~: Thermal Characterization Fixture – Tandem DUAL-SLOT Version

Following are the specific test procedures:

1. Install the card under test in one of the test setups or fixtures shown in Figure 10-2~~Figure 10-2~~~~Figure 10-2~~ to Figure 10-4~~Figure 10-4~~~~Figure 10-4~~ according to the card volumetrics.
2. Place the test setup in a thermal chamber and adjust the chamber temperature such that the card's inlet temperature is 45 °C (for both ~~300~~ 300 W and ~~225~~ 225 W cards).
3. Thermal characteristic measurements listed below should be carried out with the card in idle and full power states. The "idle" and "full power" states are defined by the add-in card vendor and are to be recorded as condition under which the thermal characterization is performed.
   – Critical component temperatures
   – Critical temperature limits
   – Inlet temperature
   – Exhaust temperature

– Fan speed

Airflow (CFM) exiting the rear I/O bracket is of great interest and value to system builders. When requested, card vendors should work directly with system builders on the details of how to measure the CFM.

10.3. Acoustic Management

The acoustic emission of a system is increasingly important for computer systems. This is becoming more challenging with higher power systems. The acoustic noise sources in a system are typically the cooling fans, the power supply fan, the graphics card fan, the hard drive, and the optical drives.

The high power card manufacturers, the chassis designers, and the system integrators must work closely together to deliver a reasonable solution, such that the end user experience is not impacted.

10.3.1. Background and Scope

The acoustic noise generated by high power PCI Express cards can be a significant contributor to overall system noise and, in fact, can be the loudest single component in the computer system. Card and system vendors will need to work together to make sure the acoustic emissions meet end-user requirements, contractual requirements, and/or government-mandated acoustic standards.

This specification does not define acoustic requirements for card compliance. Instead, this specification lists a few general guidelines and defines a standardized method for measuring card acoustics. This standardized method is intended to help system and card vendors to understand acoustic performance of the cards and to work together more efficiently and reduce acoustic emissions.

10.3.2. Card Acoustic Characterization Procedure

The following method uses an industry-standard method, ISO 3744, to measure acoustic emissions and adapts it to the particular constraints associated with PCI Express cards. This method uses the "idle" and "full power" fan speed data gathered in the Card Thermal Characterization Procedure (see Section 10.2).

1. Measurement and test setup should be as defined in ISO 3744, Acoustics – Determination of Sound Power Levels of Noise Sources Using Sound Pressure – Engineering Method in an Essentially Free Field Over a Reflecting Plane.
2. Place the card in the acoustic chamber by itself, in free air, without the system board or any other system components. The card under test should be suspended by some type of "bungee cords" to avoid any fixturing effect on acoustics. The detailed implementation of the "bungee cords" is up to each card manufacturer.
3. It is not necessary to fully power or operate the card. Instead, it is necessary to operate only the fan; this can be accomplished with an external power source and fan control circuit.

4. Measure and/or calculate the following acoustic emissions at both the "idle" and "full power" fan speeds.

   – Sound pressure, L_{PA}

   – Sound power, L_{WA}

   – 1/3-octave acoustic spectral content

Notes: IMPLEMENTATION NOTE

Acoustic Characterization

Any equipment used for fan power and control must be located outside the acoustic chamber or be sufficiently quiet so as not to contribute to the acoustic measurements.

The particular circuit (i.e., waveform) used to control the fan may have a significant effect on the acoustic results, especially at low fan speeds.

Formatted: Font: Arial Black

Formatted: Font: 14 pt, Not Bold, Not Highlight

Formatted: Not Highlight

Formatted: Left, Indent: Left: 0", Hanging: 0.38", Space Before: 12 pt, After: 0 pt, Line spacing: At least 12 pt

Formatted: Left, Space Before: 3 pt, After: 0 pt

Formatted: Font: 11 pt

Formatted: Line spacing: single

10.3.3. Acoustic Recommendations and Guidelines

In addition to minimizing the overall acoustic levels, the following points should be considered:

- The acoustic emissions should not include any prominent tones.
- Certain frequencies are more objectionable to humans than others.
- The card's fan(s) should be dynamically controlled to minimize noise over the complete range of expected operational and environmental conditions.
- The card's fan(s) should be controlled such that there are no abrupt changes or noticeable oscillations in acoustic levels or quality.
- The chassis should be designed so as to minimize coupling of vibrations and acoustic noise from the card to the chassis.
- The card should be designed so as to minimize coupling of vibrations from the card's fan to the card.

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

A

A. Insertion Loss Values (Voltage Transfer Function) (Informational Only)

The maximum loss values in dB (decibels) are specified for the system board and the add-in card. The insertion loss values are defined as the ratio of the voltage at the ASIC package pin (Transmitter/Receiver) and the voltage at the PCI Express connector interface, terminated by 100 Ω differential termination, realized as two 50 Ω resistances. These resistances are referenced to ground at the interface (see Figure A-1).

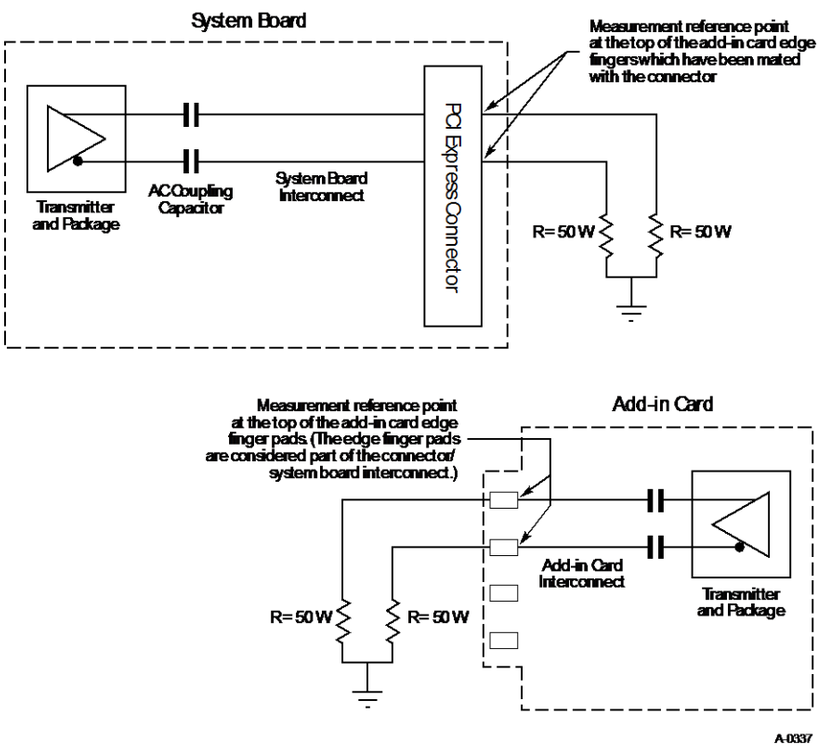


Figure A-1: Example Interconnect Terminated at the Connector Interface

All PCI Express differential trace pairs are required to be referenced to the ground plane. The loss values associated with any riser card interface and adjoining connector implementation must collectively meet the system board loss budget allocations and associated eye diagrams.

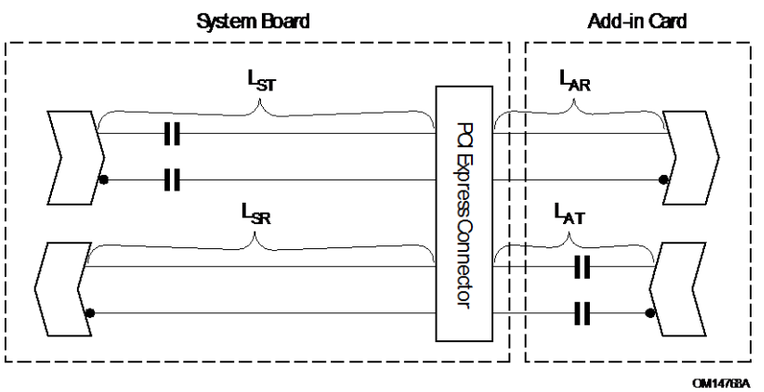


Figure A-2: Insertion Loss Budgets

Table A-1: Allocation of Interconnect Path Insertion Loss Budget for 2.5 GT/s Signaling

Loss Parameter	Loss Budget Value at 1.25 GHz (dB)		Loss Budget Value at 625 MHz (dB)		Comments
PCI Express Add-in Card	L_{AR} < 2.65	L_{AT} < 3.84	L_{AR} < 1.95	L_{AT} < 2.94	Notes 1, 2
System Board and Connector	L_{ST} < 9.30	L_{SR} < 8.11	L_{ST} < 6.00	L_{SR} < 5.01	Notes 1, 3
Guard Band	1.25		1.25		Note 1
Total Loss	L_T < 13.2		L_T < 9.2		

Notes:

1. All values are referenced to 100 Ω, realized as two 50 Ω resistances. The loss budget values include all possible crosstalk impacts (near-end and far-end) and potential mismatch of the actual interconnect with respect to the 100 Ω reference load.
2. The *PCI Express Base Specification, Revision 4.0* allows an interconnect loss of 13.2 dB for 1.25 GHz (non de-emphasized) signals and 9.2 dB for 625 MHz (de-emphasized) signals. From this, a total of 1.25 dB is held in reserve as guard band to allow for any additional attenuation that might occur when the add-in card and system board are actually mated. The allocated loss budget values in the table directly correlate to the eye diagram voltages in Section 4.8. Tradeoffs in terms of attenuation, crosstalk, and mismatch can be made within the budget allocations specified.
3. As a guide for design and simulation, the following derivation of the budgets may be assumed for 1.25 GHz signals: 5.2 dB is subtracted from 13.2 dB to account for near-end crosstalk and impedance mismatches. Out of this, the 1.25 dB is reserved as guard band. The following loss allocations are then assumed per differential pair: L_{AR} = 1.4 dB;
L_{AT} = 1.8 dB; L_{SR} = 6.2 dB; L_{ST} = 6.6 dB. These allocation assumptions must also include any effects of far-end crosstalk. 625 MHz values may be derived in a similar manner.

4. The add-in card budget does not include the add-in card ~~edge finger~~edge-finger or connector. However, it does include potential AC coupling capacitor attenuation on the Transmitter (TX) interconnect on add-in card. ~~Note that t~~The budget allocations generally allow for a maximum of 4-inch trace lengths for differential pairs having an approximate 5-mil trace width. No specific trace geometry, however, is explicitly defined in this specification. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.
5. The system board budget includes the PCI Express connector and assumes it is mated with the card ~~edge finger~~edge-finger. Refer to Section 6.3 for specifics on the standalone connector budget. The system board budget includes potential AC coupling capacitor attenuation on the Transmitter (TX) interconnect on the system board. The subscripts of the symbol designators, T and R, represent the Transmitter and Receiver respectively.

~~Note:~~ IMPLEMENTATION NOTE

Insertion Loss Budget

The insertion loss budget distributions above are used to derive the eye diagram heights as described in Section 4.8. However, they are provided here only as a design guideline. Compliance measurements must actually be verified against the eye diagrams themselves as defined in Section 4.8.

The *PCI Express Base Specification, Revision 4.0* provides design guidelines for channels designed to support 5.0 GT/s signaling.

Formatted: Not Highlight

Formatted: Indent: Left: 0", Hanging: 0.38", Space Before: 12 pt, After: 0 pt, Line spacing: At least 12 pt

Formatted: Font: 11 pt, Bold

Formatted: Indent: Left: 0", Space Before: 3 pt, After: 0 pt

B

B. 8.0 GT/s Test Channels

The 12 port s-parameters for the System-Board Test Channel with and without a standard connector/edge-finger model are distributed with this specification in the following files:

- system_board_test_channel_with_connector_8G.s12p
- system_board_test_channel_without_connector_8G.s12p

The 12 port s-parameters for the Add-in Card Test Channel with and without a standard connector/~~edge finger~~edge-finger model are distributed with this specification in the following file:

- add_in_card_test_channel_with_connector.s12p

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

16.0 GT/s Test Channels

The 12 port s-parameters for the System-Board Test Channel with and without a standard connector/edge-finger model are distributed with this specification in the following files:

- system_board_test_channel_with_connector_16G.s12p
- system_board_test_channel_without_connector_16G.s12p

The 12 port s-parameters for the Add-in Card Test Channel with and without a standard connector/~~edge finger~~edge-finger model are distributed with this specification in the following file:

add_in_card_test_channel_with_connector.s12p

Formatted: Indent: Left: 0", Hanging: 0.19", Bulleted + Level: 1 + Aligned at: 0" + Indent at: 0.25"

C

11. Acknowledgements

The following persons were instrumental in the development of the *PCI Express Card Electromechanical Specification*:[5].

Richard Allirot	Hewlett-Packard Company
Bob Atkinson	Tyco International, Ltd.
Ed Boeckmann	3Dlabs, Inc. Ltd.
Sarah Boen	Tektronix
Jason Bradley	Intel Corporation
Jim Brewer	Dell Computer Corporation
Steve Bright	Tektronix
James Bullington	3Dlabs, Inc. Ltd.
Raymond Chin	Hewlett-Packard Company
Michael Cheong	Molex Incorporated
KengYin Chok	Molex Incorporated
Dr. Jason Chou	Foxconn Electronics, Inc.
Justin Coppin	Hewlett-Packard Company
Don Craven	Intel Corporation
Dave Davitian	Tyco International, Ltd.
Bassam Elkhoury	Intel Corporation
Ikuo Enomoto	Tyco International, Ltd.
David Farmer	3Dlabs, Inc. Ltd.
Don Faw	Intel Corporation
Dan Froelich	Intel Corporation
George Hayek	Intel Corporation
Dave Helster	Tyco International, Ltd.
Ted Holden	Intel Corporation
Carl Jackson	Hewlett-Packard Company
Brian S. Jarrett	Intel
Mike Krause	Hewlett-Packard Company
Keith Lang	Molex Incorporated
Doron Lapidot	Tyco International, Ltd.
Cliff Lee	Intel Corporation
Mike Li	Wavecrest
Jit Lim	Tektronix
PT Lim	Molex Incorporated
Jasmine Lin	AMD
Dave Moss	Dell Computer Corporation
Jay Neer	Molex Incorporated
Scott Noble	Intel Corporation
Ta-Wee Ong	Molex Incorporated
Nima Osqueizadeh	AMD
John Pescatore	Dell Computer Corporation
Edmund Poh	Molex Incorporated
Curt Progl	Dell Computer Corporation
Eddie Reid	Intel Corporation
Steve Reinhold	Tektronix
Martha Rupert	FCI
Rodrigo Samper	IBM Corporation
Bill Sauber	Dell Computer Corporation
Rick Schuckle	Dell Computer Corporation
Joe Sekel	Dell Computer Corporation
Kalev Sepp	Tektronix
Joanne E. Shipe	Foxconn Electronics, Inc.
Dave Sideck	FCI
Chuck Stancil	Hewlett-Packard Company
John Stuewe	Dell Computer Corporation
Tom Sultzer	FCI
Toru Tamaki	Tyco International, Ltd.
Junichi Tanigawa	Tyco International, Ltd.
Clay Terry	3Dlabs, Inc. Ltd.
SY Theng	Molex Incorporated
Alok Tripathi	Intel Corporation
Andy Vasbinder	FCI
Gary Verdun	Dell Computer Corporation
Andy Volk	Intel Corporation
Jim Waschura	Tektronix
Clint Walker	Intel Corporation
Marc Wells	Intel Corporation
Chris Womack	Hewlett-Packard Company

[5] Company affiliation listed is at the time of specification contributions.

Yun Ling	Intel Corporation
Howard Locker	IBM Corporation
Eric Lotter	NVIDIA
Alan MacDougall	Molex Incorporated
Bob Marshall	FCI
Mike Miller	IBM Corporation
Mike Woren	Tyco International, Ltd.
Yoshisha Yamamoto	Tyco International, Ltd.
Dave Zenz	Dell Computer Corporation
Lin Zhang	AMD